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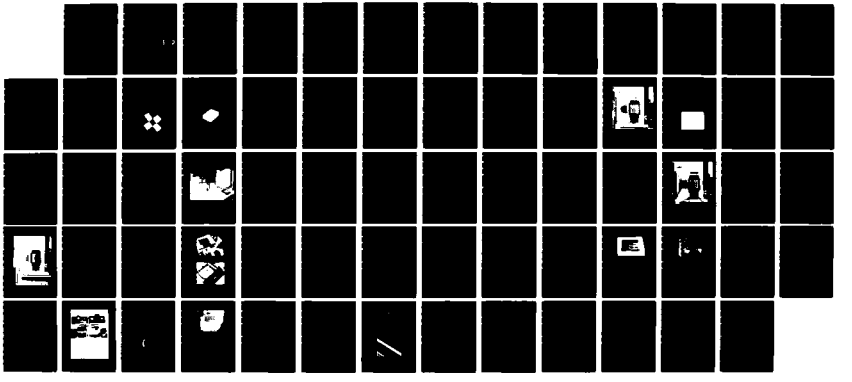

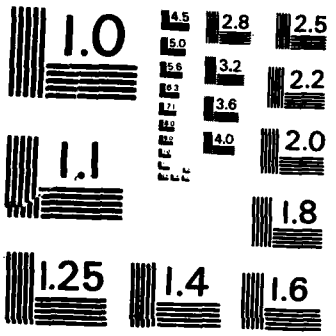

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AD-A166 458

MINIATURE FLAT PANEL DISPLAY FEASIBILITY MODEL

FINAL TECHNICAL REPORT FOR THE PERIOD July 1, 1978 through September 30, 1981

CONTRACT NO. DAAK70-78-C-0123

Prepared for

Night Vision & Electro-Optical Labs
Ft. Belvoir, VA 22060

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Principal Investigator
(805) 373-4180

NOVEMBER 1985

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Development efforts towards producing a matchbox-size miniature TV system using a thin film electroluminescence (TFEL) display are summarized. Potential applications include thermal weapons viewing sight and low mass head-mounted display systems. Results of the program include high density TFEL display surface (692 x 540 pixels at 500 lines/inch density), high density interconnect to display surface, and techniques for fabricating high density polyimide/copper hybrid circuits to provide an integrated miniature display system package. Procurement of high voltage driver ICs was a major hurdle. Upon receipt of these ICs TV imagery was demonstrated on a compact breadboard system using a 320 x 250 pixel TFEL display with 250 lines/inch resolution. Breadboard power measurements indicate a power requirement of 2.4 watts using existing components or 1.7 watts with improvement in the IC driver chip.

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1.0 INTRODUCTION AND SUMMARY

This report summarizes results of an extended program at the Rockwell Science Center directed towards producing a miniature television display system using thin film electroluminescent technology (TFEL). The goal of the program was to demonstrate feasibility of a low power miniature TV system which would capitalize on the stable TFEL solid-state emitter. Such a system would have application as the output device for many different military imaging systems where the inherent characteristics of the solid state emitter were important (temperature, shock, vibration immunity, electronic speed of response, low power operation, and reliability). Eventual potential applications include thermal imaging viewer and head-mounted display systems.

During this program, techniques were devised for producing 500 lines per inch resolution displays with 680 × 520 pixels, high definition hybrid surfaces capable of direct interconnect with the display device, and techniques for implementing the high definition interconnect required for such a miniature system. Initial results with a coarse resolution 100 × 100 display surface demonstrated the utility of even a coarse resolution device for moving objects in a television scene.

A major hurdle to producing the high density display system was procurement of high voltage driver arrays capable of modulating the TFEL display. Subsequent funding by the U.S. Army (ERADCOM) outside of this program did result in high voltage IC arrays capable of shades-of-gray modulation. When these became available, a miniature display breadboard system was assembled under Rockwell funding with 320 × 250 elements over the nominal 1 in. display surface. Measurements on this system indicate that a matchbox size TV display system should be possible using the TFEL technology with a display brightness of 10 ft.L and power consumption of less than 2.4 W. Further refinement in the display driver IC should lower the power requirement to less than 1.7 W for such a system.

This report details the investigation of extending the state-of-the-art in TFEL display resolution, high definition hybrid circuitry and high definition interconnect technology as required in order to make a matchbox size display system possible. Electro-optic measurements and power consumption figures are detailed for the miniature operating system. Finally, conclusions and recommendations are included for decreasing the power consumption and optimizing the emitter surface so that a diffraction optics type of head-mounted display system could be implemented.

2.0 BACKGROUND OF DEVELOPMENT OF MINIATURE TFEL DISPLAY SYSTEM

Initial efforts under a prior contact (DAAK70-77-C-0141) demonstrated for the first time that resolution as high as 500 lines per inch could be achieved with the TFEL technology. This work showed that 8 μm wide gaps between parallel conductors were adequate to provide isolation in the matrix display so that negligible crosstalk resulted between adjacent electrodes. Also, etching techniques were worked out which allowed this high definition patterning of both the ITO transparent conductive layer as well as the rear aluminum electrode pattern. Brightness as much as 10 ft.L was measured under 1/500 duty cycle using existing state-of-the-art TFEL materials. That effort did yield a 100 × 100 active matrix display over a 0.1" × 0.1" area.

Subsequent effort under the present contract was directed toward producing 500 lines per in. resolution over a nominal 1 in. display area so that a television image of 680 × 540 elements could be produced. Specific areas addressed in this effort included techniques for uniformly etching the address lines on the display surface over the larger areas (nominally 1 in. square) with minimum blemishes, techniques for electrically accessing these high resolution electrode patterns, and techniques for providing high-density hybrid drivers to be attached to the display so that a compact miniature display system would result. At the onset of the program, it appeared that an existing technology could provide the high voltage drivers required for the high-density hybrid electronics. However, further testing indicated that the dielectrically isolated bipolar devices were not adequate and another technology (DMOS) was selected for development of a custom multichannel high voltage driver IC. Considerable effort was expended by the vendor (Supertex) with respect to the limited funding under subcontract from this program. Eventually, high voltage arrays did become available as a result of U.S. Army funding under other programs to Supertex. These multichannel ICs are capable of video modulation of the TFEL display. At this point, Rockwell, under their own funding, implemented a reduced resolution system (250 lines per inch) that

contained 320 × 240 elements and did show video modulation using these new high voltage transistor arrays.

The evolution of the efforts under this program first demonstrated a coarse resolution of 32 × 32 elements in the 1 in. active area using discrete transistor drivers for the electronics. Shades of gray and uniformity were measured with this device. Next, a 100 × 100 matrix over a 1 in. area was developed and demonstrated, again using discrete transistors for drivers. Results of this effort showed that for dynamic scenes in which the image was moving, the 100 × 100 resolution was surprisingly useful. Also, the display was driven using ribbon cables that interconnected between breadboard electronics and the drive surface. This demonstrated that the display could be remoted from the electronics, if necessary, to provide a very low mass display surface.

Other efforts under this program did provide means for high density interconnect between the display surface and the IC drivers contained on a separate hybrid electronics surface. Also, techniques were developed for producing high definition multilayer copper polyimide hybrid surfaces as required for direct attachment of driver IC arrays and interconnection to the display surface. High voltage column drivers capable of shades of gray modulation finally became available. Based on power measurements made with the more recent 320 × 240 (250 lines per inch) breadboard system, it appears practical to fabricate a system which meets most of the operating goals of the contract with less than 2.4 W power consumption.

3.0 MINIATURE FLAT PLANEL DISPLAY SYSTEM DESIGN

3.1 Feasibility Model Design Requirements and Goals

3.1.1 Pixel Density (p/mm) * 20

3.1.2 Format

(1) Vertical Pixels (#) *512

(2) Horizontal Pixels (#) *683

3.1.3 Package Size

(1) Vertical (mm) Goal < 45

(2) Horizontal (mm) Goal < 55

(3) Depth (mm) Goal < 15

3.1.4 Electronics

(1) TV compatibility *525 line composite TV

(2) Display Panel/Electronics interface

(3) Voltage - to display (V) Goal < 200

(4) Power - total watts at 35 cd/m^2 Goal < 1/2

3.2 Feasibility Model Performance Requirements and Goals

3.2.1 Luminance, broadband - average luminance at maximum output (cd/m^2). * 35 Goal > 1,000

3.2.2 Luminance Narrowband - average luminance at maximum output with a 50Å half-power bandwidth cd/m^2 Goal > 1,000

3.2.3 Luminance Scale - # of $\sqrt{2}$ luminance steps with display set at the peak and 1/4 of the peak output (#) *8 Goal > 16

3.2.4 Nonuniformity - measured at maximum and at 1/4 maximum luminance (% of highest luminance)

(1) Overall	200 Goal < 10
(2) Adjacent Pixel	30 Goal < 5

3.2.5 Response - luminance integrated over the frame following turn off or on (% of maximum luminance)

(1) Maximum luminance to off	Goal < 10%
(2) Off to maximum luminance	Goal > 90%

* Minimum requirement

3.3 Package Design

Figure 3.3-1 illustrates the approach taken toward providing the miniature TV system. The thin film EL display surface is contained on the outer glass substrate. The electronic drivers and video processing circuitry are contained in the hybrid packages. Figure 3.3-2 is a rear view showing the hybrid drivers unfolded. Figure 3.3-3 shows how the hybrids are interweaved upon folding. The system assembly is mounted in a rigid case as shown in the drawing of Fig. 3.3-4. The substrate for the hybrid package consists of a copper-clad polyimide foil in which the copper is etched to provide the appropriate conductor pattern. These same etched conductor lines continue out from the hybrid package on the interconnecting flap which is an integral part of the hybrid itself. In the area of the hybrid package, an aluminum heat sink plate is bonded to the kapton material in order to provide heat dissipation as well as a stiff bonding surface for the IC chips located within the hybrid. The extending flap provides a flexible means of interconnecting to the display surface. Each driver package is folded behind the display so that a minimum display volume results. The case contains a front window which is hermetically sealed to the metal side of the can. The display and driver

electronics are inserted through the back of the case. The heat sinks of the hybrid drivers have an L-shaped leg at two opposite edges to make good thermal contact to the case. In the cross section view in Fig. 3.3-4, only one leg for the driver heat sink is shown. The opposite leg is notched to allow for passage of the polyimide interconnect to the display surface and so does not appear in the cross section. The notched leg contacts the out case at the corners of the case and so provides a spring fit for the hybrid substrate into the case. In the final assembly step the rear cover is soldered in place on the case, thus providing a hermetic seal for the display system. A hermetic feedthrough on the side of the display provides for the video signal input as well as the low-voltage and high-voltage requirements for the driver electronics. The power supply module, which is not shown in the drawing, is connected by a single umbilical cord and so can be located at a convenient location for the user.

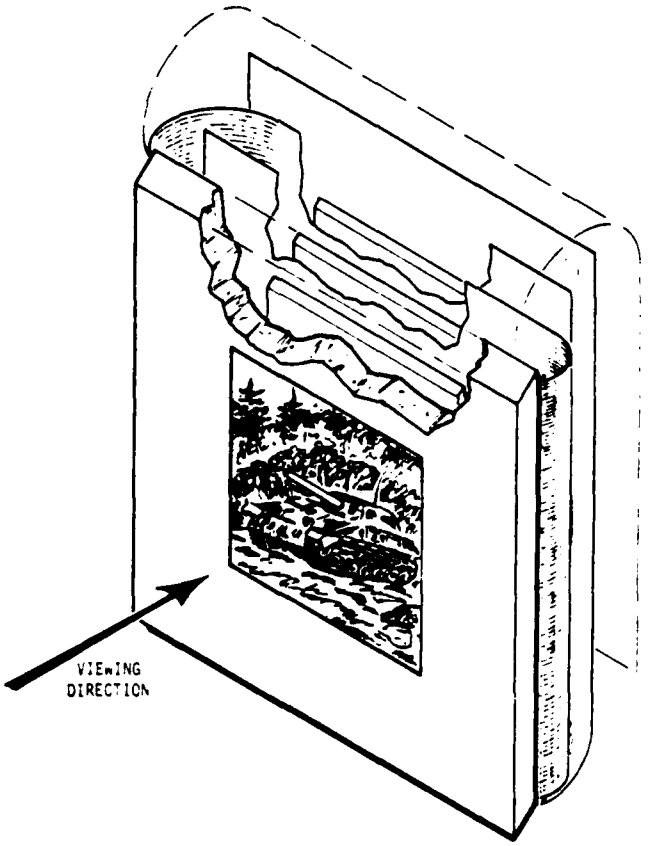

Fig. 3.3-1 Miniature flat panel display system.

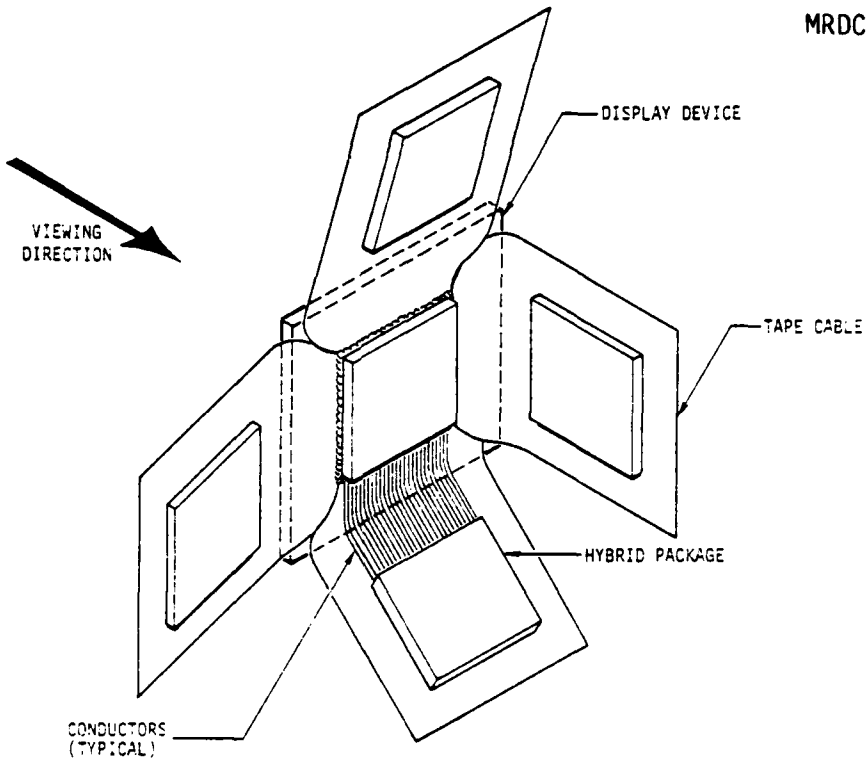

Fig. 3.3-2 Rear view of unfolded display system.

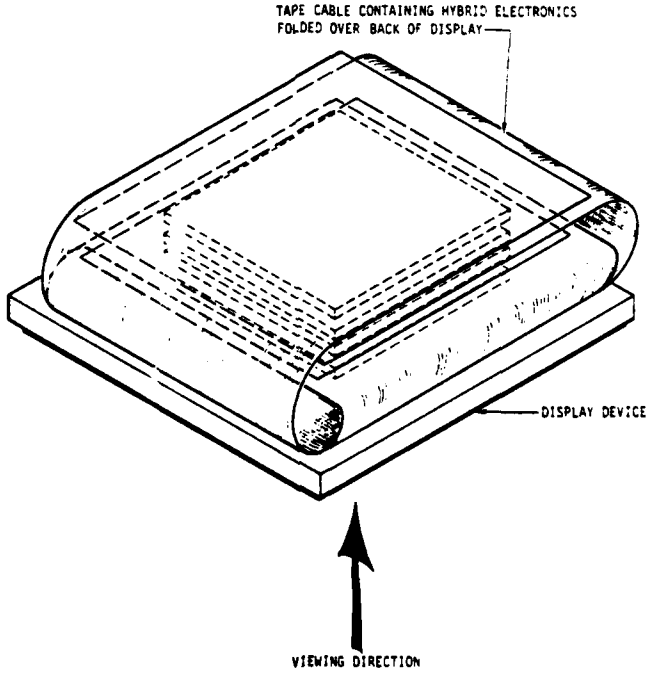

Fig. 3.3-3 Rear view of folded display system.

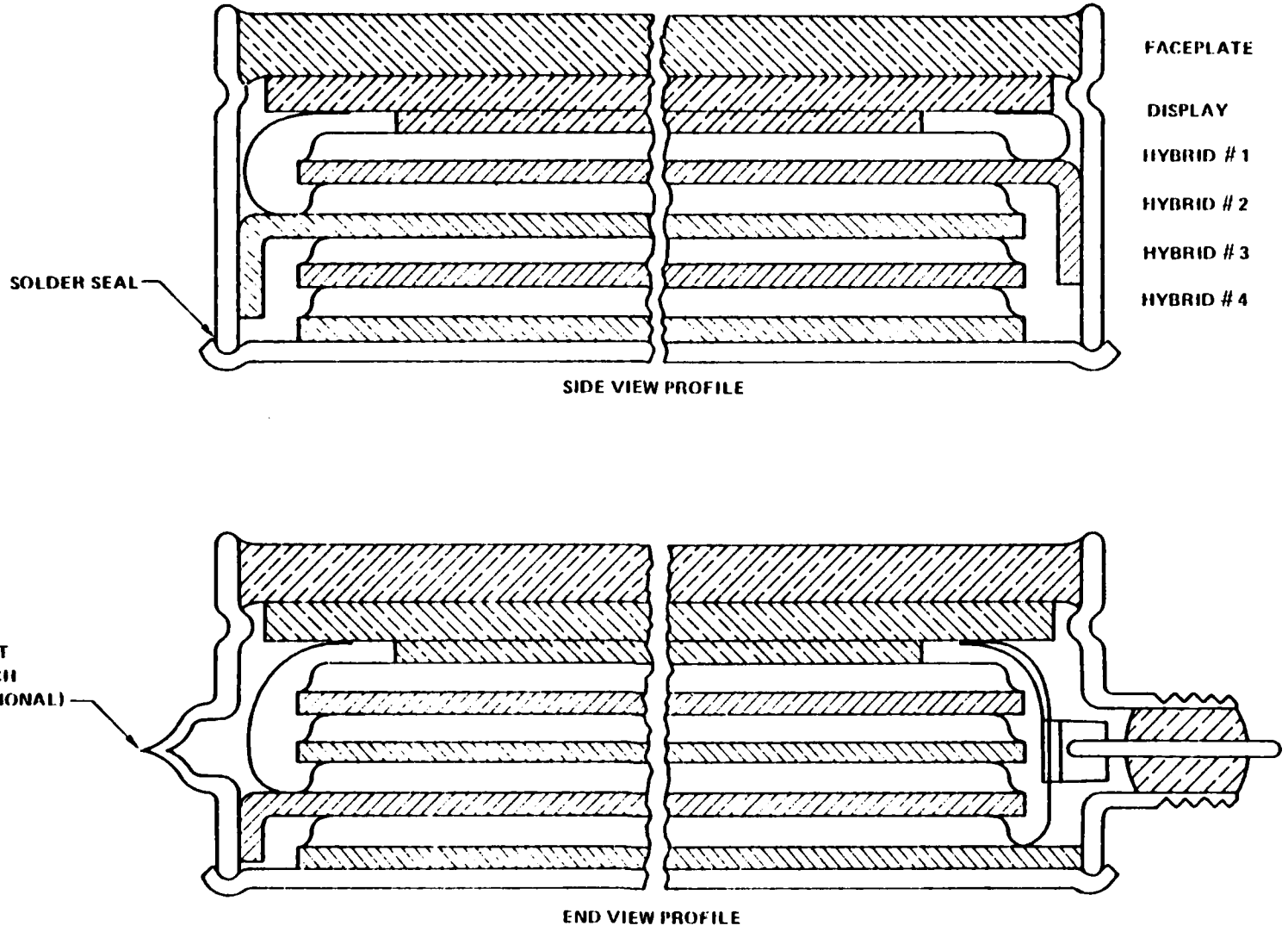

Fig. 3.3-4 Display system package.

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In order to check the concept of the interweaved hybrid packages, a mock-up was constructed using the actual dimensions as required for the miniature flat panel system. Figure 3.3-5 is a picture of this mock-up in the unfolded state and Fig. 3.3-6 is a picture in the folded state without any external hermetic package. The mock-up used the copper-clad polyimide material that will be used as the final hybrid substrate. The mock-up showed that adhesion of the polyimide to the glass display surface appeared adequate. Also, the copper conductor material on the polyimide showed no signs of delamination or cracking after many repeated foldings and unfoldings of the assembly.

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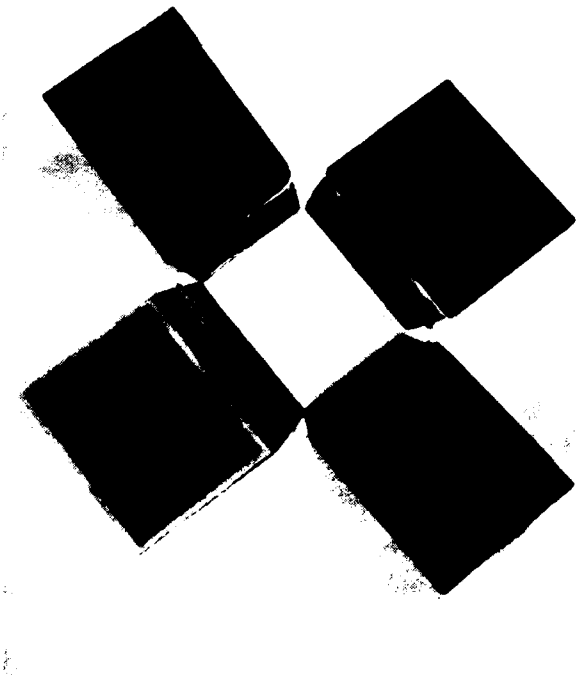

Fig. 3.3-5 Miniature flat panel EL display mock-up (unfolded).

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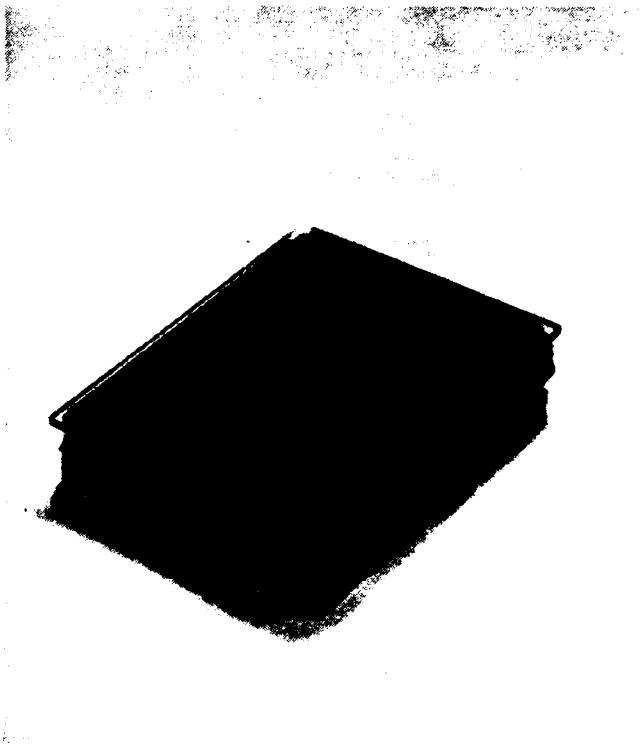

Fig. 3.3-6 Miniature flat panel EL display mock-up (folded).

4.0 DISPLAY DEVICE

Figure 4.0-1 shows a schematic cross section of the display structure and illustrates the simplicity of the thin film EL device. Etched transparent electrodes of indium oxide contained on the glass substrate form the electrode pattern in one direction. Vapor deposited layers of yttrium oxide (dielectric 1 and 2) are located on either side of the vapor deposited zinc sulfide manganese activated phosphor. The rear aluminum electrode is applied orthogonal to the original indium oxide electrodes to provide the XY addressing of the emitter elements in the matrix. A unique characteristic of this structure is the ability to selectively address the emitter element within the matrix with negligible visible cross talk from nonaddressed intersections. This is due to the highly nonlinear electro-optic response of the emitter. The nonlinear response in turn is due to the nature of electronic injection into the zinc sulfide phosphor by a tunnel emission phenomenon. The tunnel emission characteristic is relatively independent of temperature so that the display can be operated over a wide temperature range.

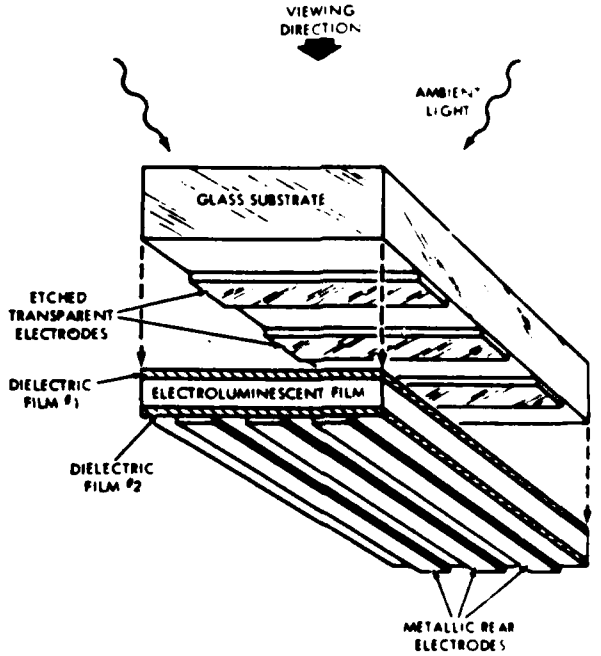

Fig. 4.0-1 Thin film emitter structure.

4.1 TFEL Emitter

The emitter material is similar to that previously reported in the final report for the miniature active matrix display.[1] Extensive electro-optic characterization is described in that report. One of the more important characteristics is the brightness-voltage response as shown in Fig. 4.1-1. This illustrates the extreme nonlinear relationship which is required for matrix addressing of the emitter so that at 1/2 voltage excitation negligible light emission occurs. Also, as much as 10 ft.L brightness is available in a 1/500 duty cycle excitation such as prevails in the miniature flat panel display system.

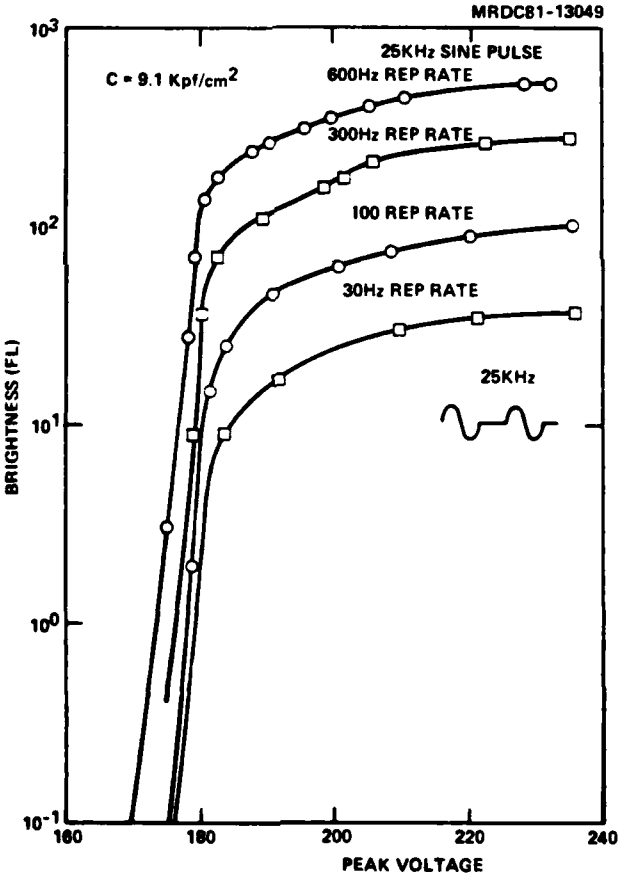

Fig. 4.1-1 Brightness vs voltage for thin film emitter under 1/500 duty cycle drive.

4.2 Electrode Design

Figure 4.2-1 illustrates the geometric layout of the display device. An art work similar to that used in the previous contract has been stepped and repeated to provide the full 520 × 690 line matrix. A spacing between parallel conductors of 8 μm and a conductor width of 42.8 μm provides the required 500 line per inch resolution. This results in a display with an active area to total area ratio of 0.71. Figure 4.2-2 is a 15X enlargement of a portion of that artwork showing contact pad areas at the edges of display. The conductor electrodes in one direction are interdigitated so that alternate electrodes are terminated on either side of the display. The contact pads on the side edges of the display consist of an array 52 pads long by 5 pads deep so that 260 contacts are possible on each side of the display in order to address 512 rows.

The overall substrate size is 51 mm × 43 mm, which will fit into the required package size (see Fig. 3.3-4). The active substrate area is protected from the ambient by a rear cover slip which is cemented into place after fabrication using a low outgassing epoxy tape material commonly used for hybrid packaging purposes. The rear cover glass also contains a porthole through which the display is vacuum pumped and baked prior to a final metal solder seal in a controlled gas ambient. As previously described, the display and associated electronics are finally sealed in a hermetic package so that water permeation through the epoxy seal of the display should not be a problem.

An important consideration in a matrix address emitter is the power loss in the transparent conductor lines through I^2R heating. The major current flow is due to the displacement current (reactive component) that couples to the nonaddressed rows during the column address time. If one assumes a capacitance of 0.1 μF for the total display area, this represents 100 Ω reactive impedance at 15 KHz frequency assumed for the column address. The peak-to-peak voltage producing this current is 100 V since the nonaddress rows are clamped to the ground. On the basis that the line is driven and the current

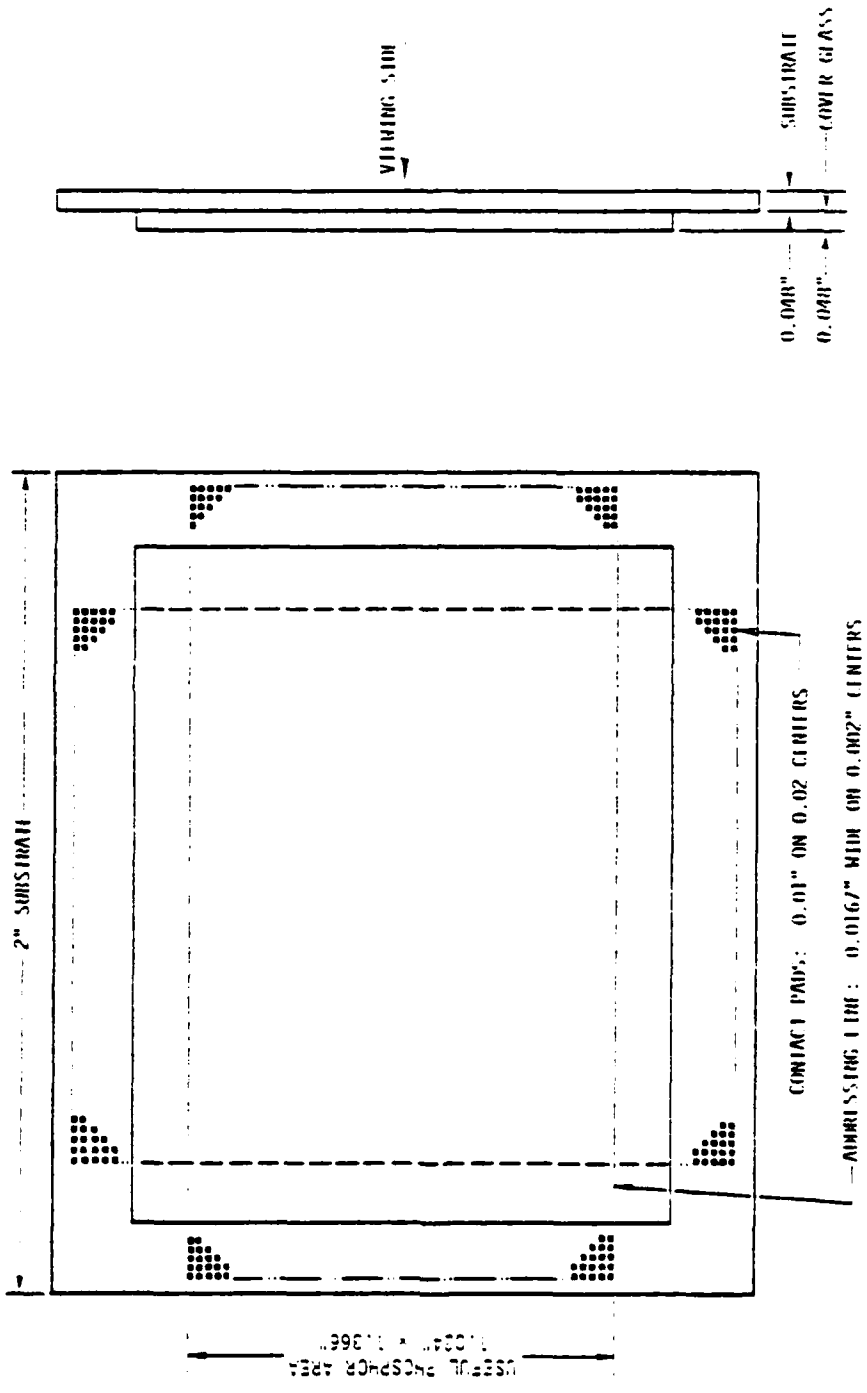

Fig. 4.2-1 Layout of display device.

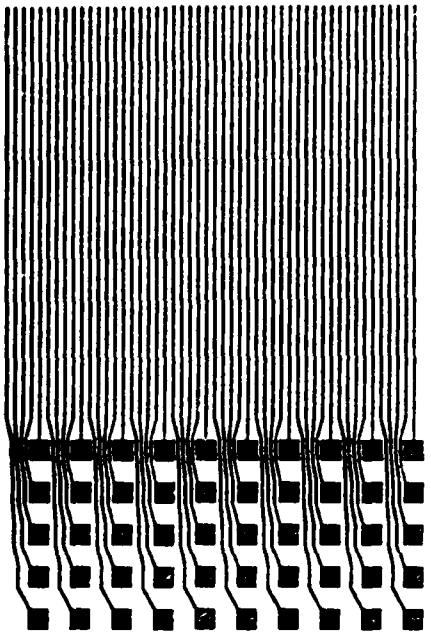

Fig. 4.2-2 15X enlargement of contact pad area and conductor pattern.

linearly decreases in the line as a function of the distance from the drive end, the power loss in the line can be shown to be $\frac{I^2R}{3}$, where I is the RMS value of the current and R is the overall resistance of the line. Taking the resistance of the whole array is parallel results in about one square of resistance or 5 Ω, assuming 5 Ω per square ITO transparent conductor. Therefore, the power loss in these conductors is $(V_{RMS}/Z)^2R/3 = (\frac{100}{2\sqrt{2}\ 100})^2\ 5/3 = 0.2\omega$. This power consumption can be reduced by another factor of two through use of a $\frac{V}{3}$ driving voltage on the columns and $\frac{2V}{3}$ on the rows.[2]

4.3 Display for Video Breadboard

In order to provide a test display for evaluation of the breadboard electronics, a number of coarse matrix displays with 32 × 32 and 100 × 100 pixels were fabricated with the same total area as the final display. The 15X

enlargement artwork, Fig. 4.2-2, was used. This provided displays for breadboard experimentation and required minimum investment in fabrication of the displays compared with the fine line version. Figure 4.3-1 is a photograph of an operating 32 × 32 display. In this case, contact to the display was made through an etched metal lead frame which was attached to the display using conductive epoxy and then reflow soldered to an adjacent printed circuit board so that conventional edge connectors could be used to rapidly connect the display to the display system. This type of display was used for initial evaluation of the breadboard electronics.

4.4 Fabrication of High Density Display (680 × 540 Elements)

4.4.1 Etching of Indium Tin Oxide (ITO) Coated Glass Substrate Material

Precoated ITO glass substrates were purchased from commercial sources. Initially, sputtered material was used typically with 15 Ω per square resistivity, 2700Å thickness. Continuing problems with this source were particulates of indium from the sputtering targets embedded in the deposited film. Subsequently, a different vendor was located who also provided a higher conductivity and a thinner layer (10 Ω per square, 2300Å thickness) and did eliminate the problem of the indium bumps in the coating. Techniques were developed for etching this material in hot hydrochloric acid so that 8 μ gaps over the required 1.3 in. span could be provided with good uniformity over the nominal 1 in. display area. The rear aluminum electrode was also defined by an etching process so that similar 8 μ gaps were obtained.

The dielectric materials (yttria) and zinc sulfide were electron beam evaporated as described in a previous report.[1]

In order to provide mechanical protection to the display surface, a rear cover glass was attached to the display using an epoxy tape seal material. Also located in the rear covered glass was a metallized porthole so that following attachment of the rear cover glass to the display through cure of

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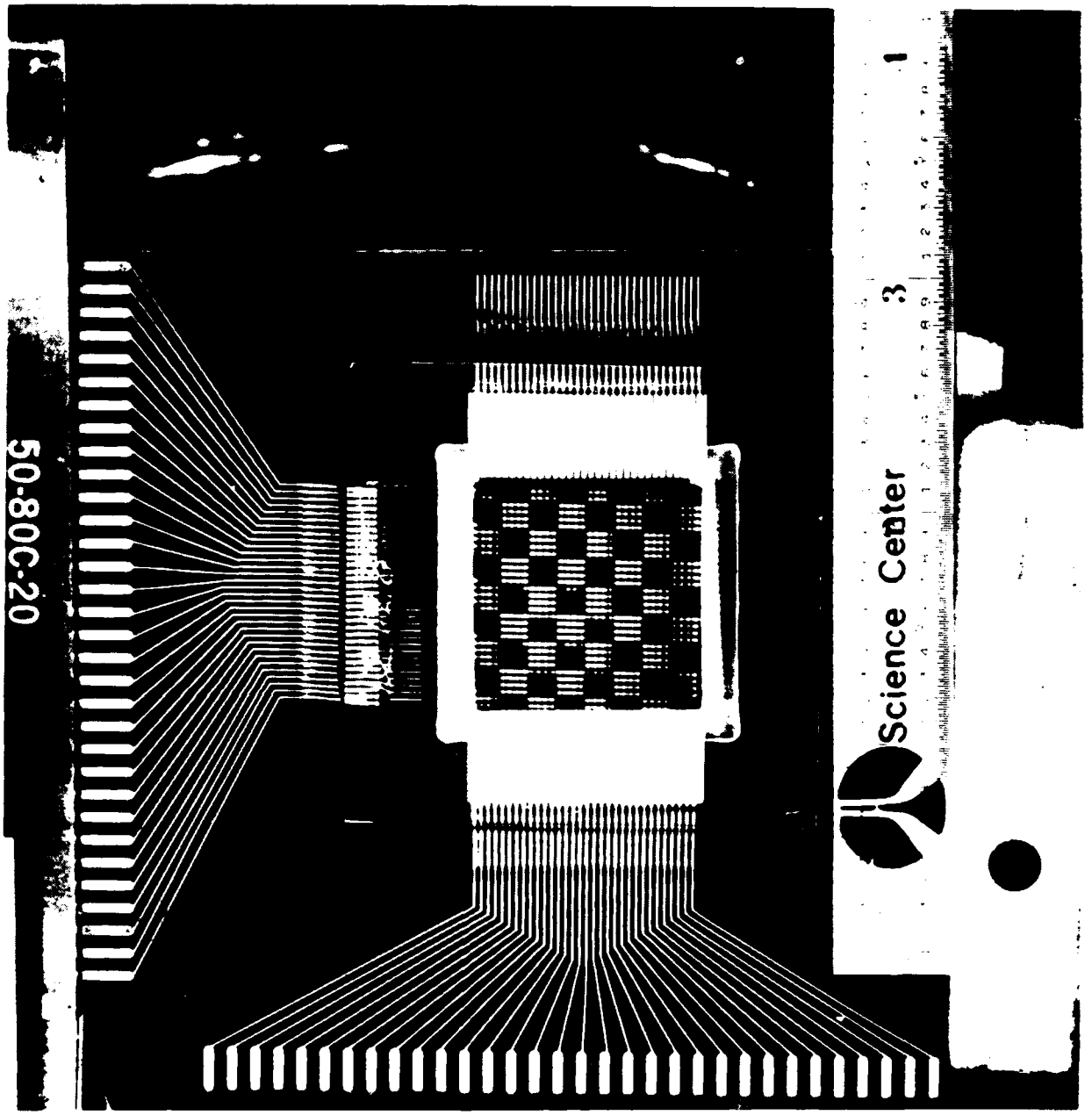

Fig. 4.3-1 Checkerboard pattern 32 × 32 display.

the epoxy tape, the display could then be sealed in a dry gas ambient inside a dry box. Final seal was provided with a brass coverplate soldered to the metallized area of the porthole. For operation under high humidity conditions, the epoxy seal of this rear cover glass is not adequate. The use of an external hermetically sealed glass-metal container was intended to provide water from effecting the display surface (see Section 3.3).

4.5 Yield Problems

Figure 4.5-1 is a picture of an operating high density display (640 × 520 elements over nominal 1 in. viewing area). In this figure every other row was not energized. A number of rows are short-circuited, as well as open circuit.

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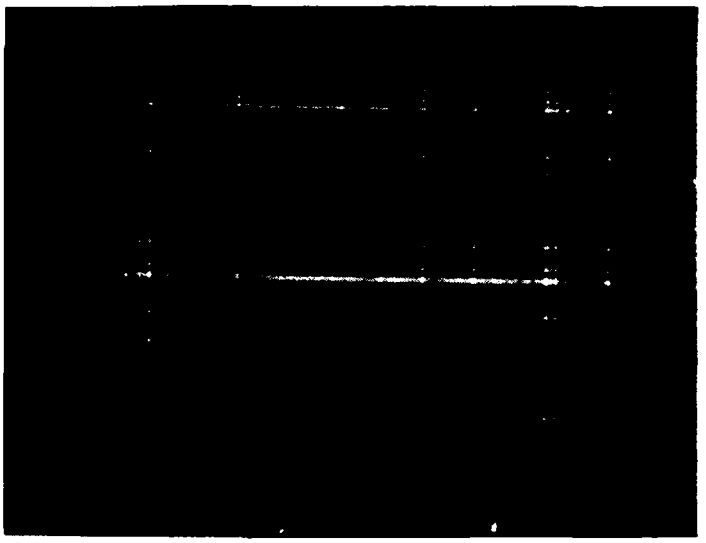


Fig. 4.5-1 Photograph of operating 640 × 520 display.

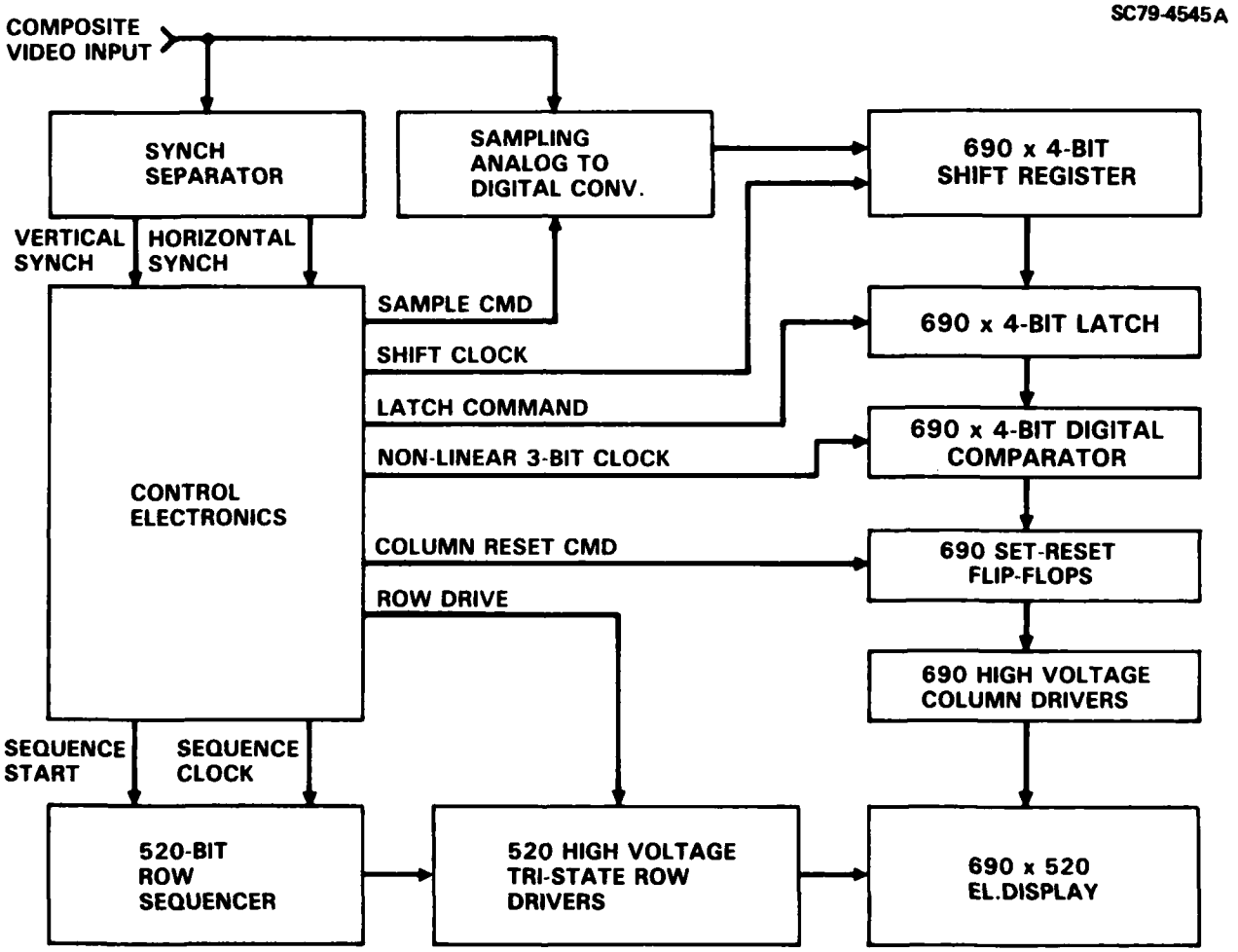
Once ITO had been received without sputtering-induced bumps of indium, the next limiting factor in yield was scratches in the coating in the received part or as process induced. Visual inspection of the part under backside illumination from a fiber optic high intensity light source revealed scratches in the ITO in the received material. Chrome glass tooling was used throughout so that scratching of the glass photo tooling was minimized. Inspection of the photoresist pattern was done manually under a microscope. Automated inspection procedures using pattern recognition equipment would be important for any mass production of this device. In the case of the aluminum electrode, bridging between adjacent electrodes was more of a problem than scratches in the electrode material itself. A focussed argon ion laser beam was used to selectively trim bridge spots in the rear aluminum electrode which were detected upon light-up of the display panel. The transparent rear cover glass allowed repair of this rear electrode after the display was sealed.

Early results with the 100 × 100 breadboard model showed that the transfer characteristic of the brightness voltage curve was important in order to reproduce shades of gray in the video. For instance, with a slope less than 5 V/decade of brightness graphics information could be presented readily, but shades of gray were difficult to reproduce. Therefore, an important characteristic for video use is a control of the slope of the brightness voltage characteristic.

5.0 VIDEO ELECTRONICS

5.1 System Design

The block diagram of the video electronics used to drive the thin film EL display is shown in Fig. 5.1-1. The matrix is addressed line at a time. All columns are addressed simultaneously while the rows are sequentially selected. The incoming composite video information is amplified and the horizontal and vertical sync pulses are separated from the composite signal. The video is fed into the A/D converter. The output of the A/D converter is a four-bit signal representing sixteen shades of gray. The four-bit signal is then fed into a serial-in-parallel-out shift register four bits at a time. After one line of information has been shifted into the register, it is stored in latches while the next line is processed. Shades of gray are generated in the display by modulating the width of the column driver pulse. At the start of a line modulation, a ramp voltage is applied to all the column drivers simultaneously. The amplitude of the ramp for a particular column is determined by the turn-off time for that column driver. In order to correct for the nonlinear brightness voltage characteristic of the display device, a nonlinear code is inserted between the A/D converter output and the stored data input on the latch for each column driver. This code can be modified according to the gamma correction requirements of a particular display surface. A four-bit code stored at each column driver is sensed by a comparator circuit at each column circuit. When the corresponding amplitude of the ramp on the column drivers matches that equivalent digital amplitude on the column latch, the driver is set into a high impedance state. During the access time for a particular line, that line is driven negative with respect to the column driver output by the row drivers. All other rows at that time are in a high impedance state and assume some intermediate voltage level as determined by capacitive coupling from the rest of the display. After scanning all the rows in a particular display, a refresh pulse is applied by simultaneously driving all rows positive while maintaining all columns clamped to zero potential level. The effect of this reverse polarity pulse to the elements of the



ELECTROLUMINESCENT VIDEO DISPLAY BLOCK DIAGRAM

Fig. 5.1-1 Block diagram of video electronics.

display is to provide the A/C waveform necessary for long-lived displays. Also a second pulse of light occurs at this time from each of the previously selected intersects within the display. Figure 5.1-2 illustrates the voltage waveforms during the address cycle.

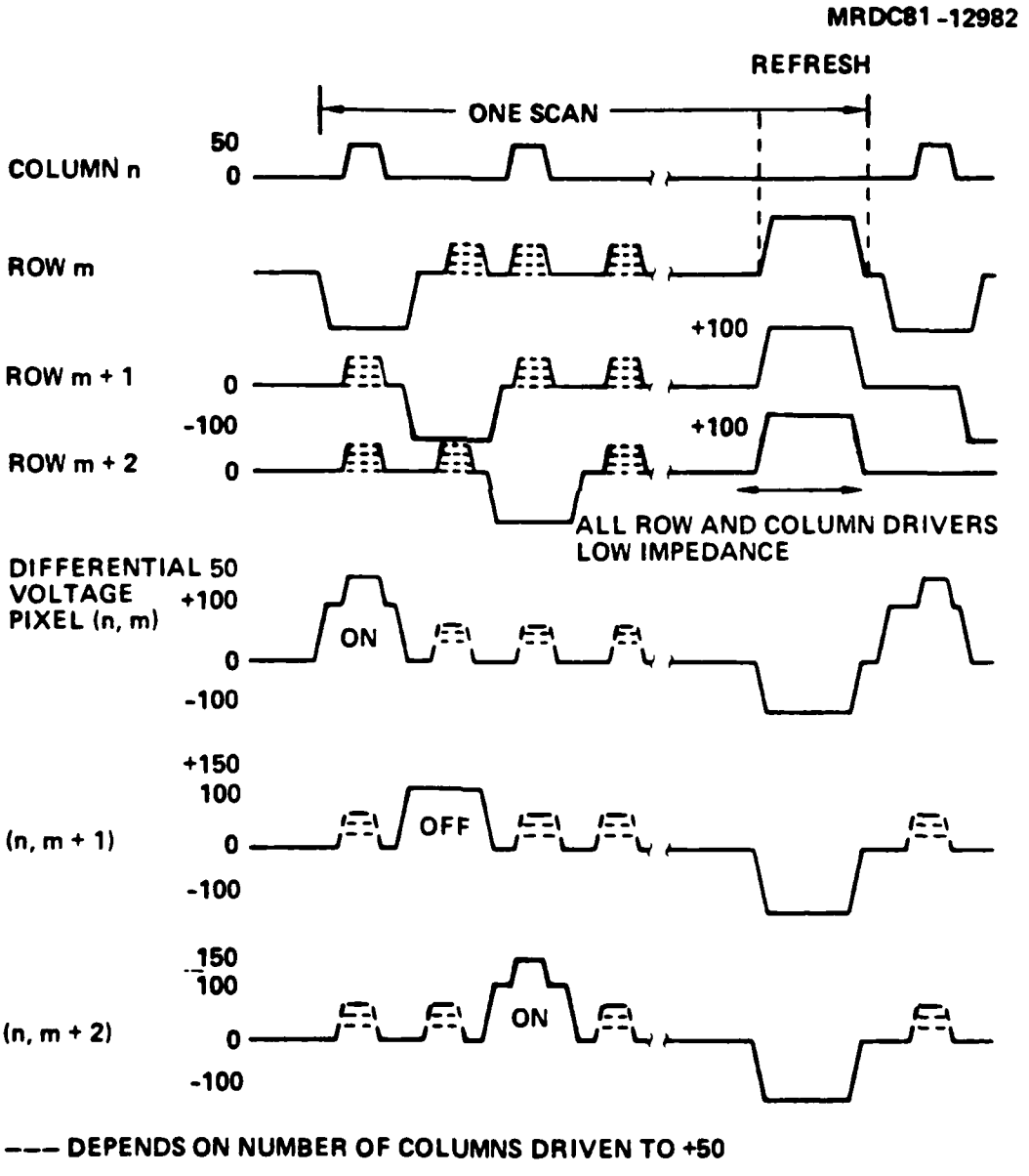


Fig. 5.1-2 Voltage waveform of matrix-addressed display.

5.2 Video Output Driver

As initially designed, the latches, comparator and logic circuit for each column channel were to be contained in a separate logic chip, the output of which fed a separate IC driver chip. In the interim, other funding by the U.S. Army for other TFEL projects did develop a video column modulation chip (Supertex HV01) which contains the shift register, latch, comparator and high voltage modulation capability on one IC. This particular IC has a capacity for 16 channels per IC.

Major pacing item in the development of this program was the availability of high voltage IC drivers, such as required for miniature packaging of the display system. Initial breadboard tests with up to 100 × 100 rows and columns in the system were conducted using discrete transistors (see Fig. 5.2-1). These tests underscored the need for IC driver outputs in terms of uniform characteristics for the transistors from column to column for uniform modulation as well as high density packaging. The first designs used a column modulation of 1/2 the drive voltage of the panel (i.e., 100 V peak). Later designs simultaneously depressed the addressed row by 100 V while applying only 50 V to the column driver in order to provide the required 150 V across the "full-on" pixel. A major concern in the output drive is minimum power dissipation while the voltage is swinging over a 50 V range. For instance, a simple output stage with a transistor collector tied to a load resistor would dissipate too much power through the load resistor in the zero voltage output state. Therefore, it was recognized that a dynamic output impedance was necessary on the driver channel such as provided by a complimentary pair of transistors or a totem pole arrangement in which one transistor of the pair is turned while the other is turned off provide the two extremes in output voltage. Figure 5.2-2 shows the complementary pair-type driver arrangement used on the initial breadboard circuit. The operation of the circuit is described as follows.

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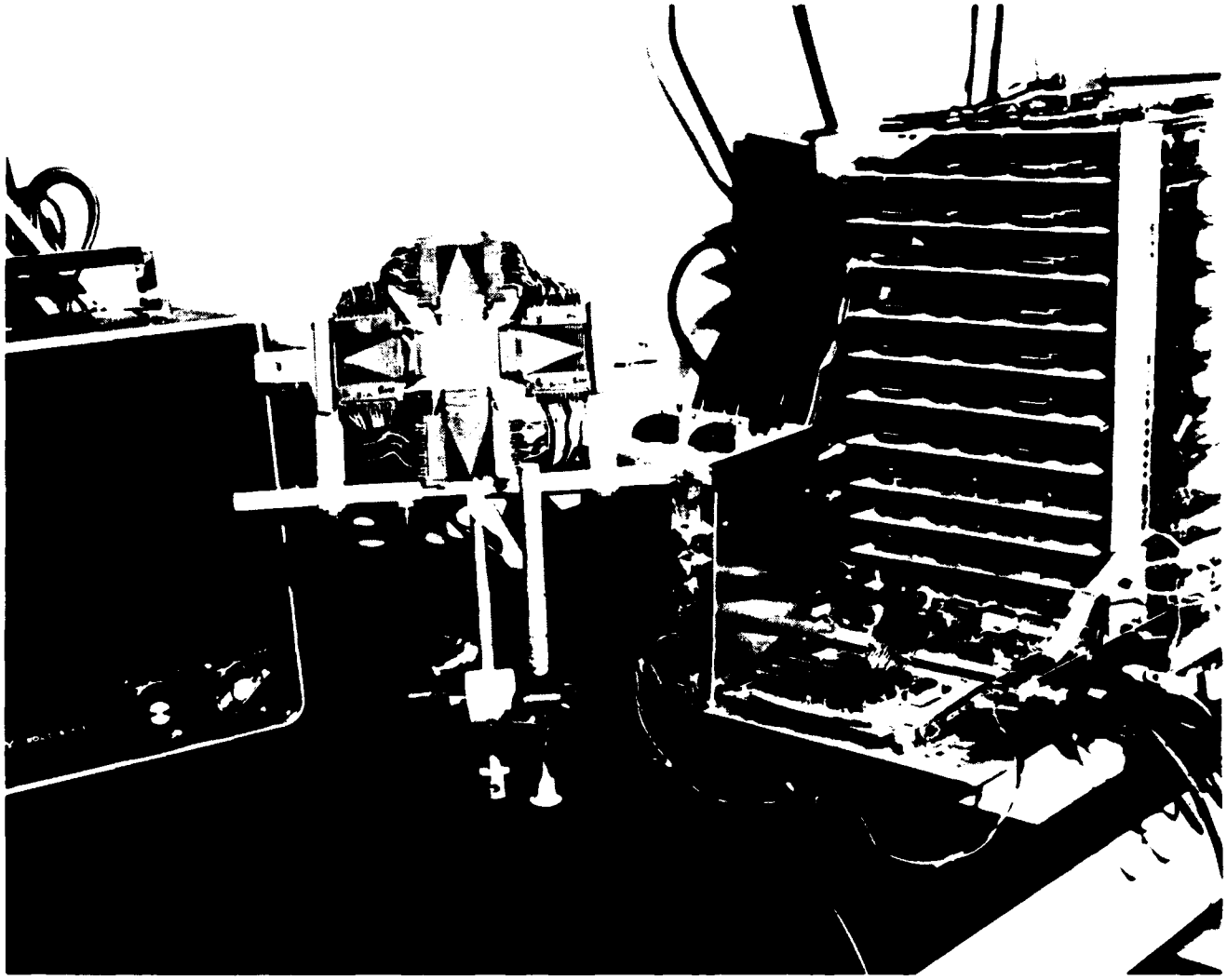
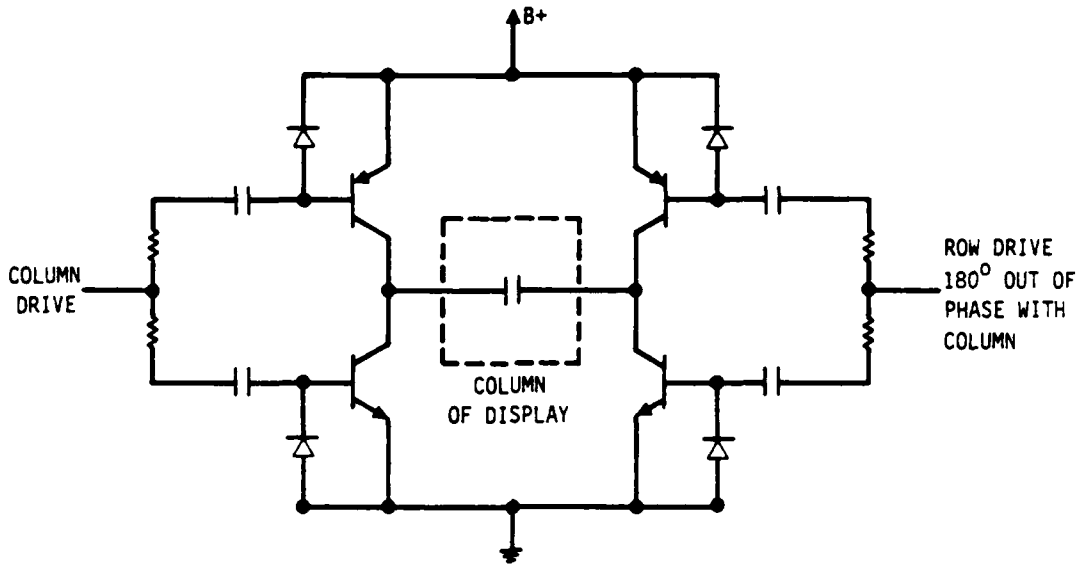


Fig. 5.2-1 Photograph of 100 × 100 element breadboard.



HIGH VOLTAGE DRIVER

Fig. 5.2-2 Complementary pair high voltage driver.

During the negative transition of the input signal, Q_1 (NPN) is conductive and Q_3 (PNP) is effectively biased off, thus connecting the row element to ground. The pulse width and amplitude of the column signal is controlled during this phase to provide the appropriate video information to each respective pixel. During the next half cycle, the phases are reversed pulling the column electrodes essentially to ground while the row elements are connected to high voltage, thus providing effective AC excitation for the display.

The nonaddressed row is in a high impedance state and pixel elements in nonaddressed rows never exceed the threshold voltage. The advantage of the complementary circuit is that no current flows in any transistor except during the interval in which the particular element is turned on, resulting in no power losses during periods when the display is not excited. The complemen-

tary pair driver is a high efficient circuit which consumes power only when useful addressing of the picture elements is required.

The circuit for Phase I was implemented using discrete transistors. This created several difficulties due to excess leakage currents of the bipolar transistors and stored charge at the base of each transistor. In order to remedy these problems, it was necessary to add additional circuitry. The excess circuitry was not required in the final version since the discrete transistors were replaced with high-voltage DMOS complementary arrays which have extremely low leakage currents and negligible stored charge at the gate of the MOS devices.

Initially it was intended to use dielectrically isolated bipolar transistors which were available at the time of the inception of the project from a commercial source. Evaluation of prototype breadboard circuitry showed that the input capacitance required because of bipolar base currents were much too large to be included on the integrated circuit chip. Conversely, in order to include the coupling capacitors on the chip, the number of transistors per chip was reduced to four. Therefore, this approach was unacceptable. A subcontracted development program was initiated with Supertex to provide high voltage DMOS IC arrays. The DMOS approach had a number of advantages over the initial bipolar approach. First, DMOS is directly compatible signal-wise to other CMOS circuitry. Secondly, the MOSFET devices have negligible leakage currents in the gates and therefore, negligible charge storage problems. This results in much smaller coupling capacitors required for voltage isolation from the logic circuitry. Another advantage is higher packing density available with the MOS processing than is possible with bipolar devices because of the dielectric isolation requirements for the bipolar ICs. Also, the more simplified MOS process results in significantly lower cost. Based on quotations for both technologies, the volume cost of the DMOS ICs was about 1/3 that of the bipolar approach.

Development work at Supertex showed that high voltage ICs could be fabricated with a DMOS process which individually met the requirements of the

program (> 350 V capacity, 20 mA capacity, 400 Ω on resistance). Initially the intent was to contain both the P and the N devices on one substrate which significantly lowers the interconnect problem on the hybrid circuit. Tests were conducted in which the N material was provided in a well set into a very deep P diffusion. However, in order to support the voltage requirements, the depth of the initial P diffusion required greater than 1 week diffusion time, which was impractical in terms of manufacture. Therefore, a second approach was finally implemented in which separate chips of both P- and N-type were fabricated on separate substrates to be eventually interconnected on the hybrid surface. This change in output driver stage had a significant impact on the hybrid layout, namely increasing the number of hybrid drive surfaces behind the display from 4 to 7 in number. Work at Supertex continued on developing the separate P and N high voltage arrays and did succeed in achieving many of the operating requirements for the ICs. Major problems were encountered in coupling the signal into the P channel IC which was at high voltage with respect to the ground signal input. Several types of isolation in the input circuit were implemented, including a junction-isolated type as well as a dielectric isolated coupling capacitor. In the case of the coupling capacitor, the area requirements for each channel increased significantly. After many iterations with changes in artwork (each iteration typically taking six weeks or more), the input coupling problem was still not solved and the required area of both the ICs and the hybrid surface had increased significantly over the original design. It should be stressed that there were no high voltage complementary pair IC arrays available at this time and this was a significant undertaking. Supertex did devote a considerable amount of their own effort in attempting to solving this problem. As previously stated, the MOS transistor characteristics were achieved. Subsequent subcontract funding by the U.S. Army did develop arrays capable of shades of gray modulation eight years after the inception of this program. Using these arrays, Rockwell did demonstrate video display on a 320 × 240 miniature display surface under their own funding.

5.3 Video Breadboard Test Results

The following data were taken with the early breadboard using a 32 × 32 element display as well as the discrete transistor driver output. Similar data has not been obtained for the more recently developed 320 × 240 display system. However, the data demonstrated the availability of shades of gray and the uniformity possible.

Figure 5.3-1 is a schematic that represents the test measuring system used to measure the display characteristics. The display for the video breadboard is described in Section 4.0. The display was connected to the video electronics through ribbon cables.

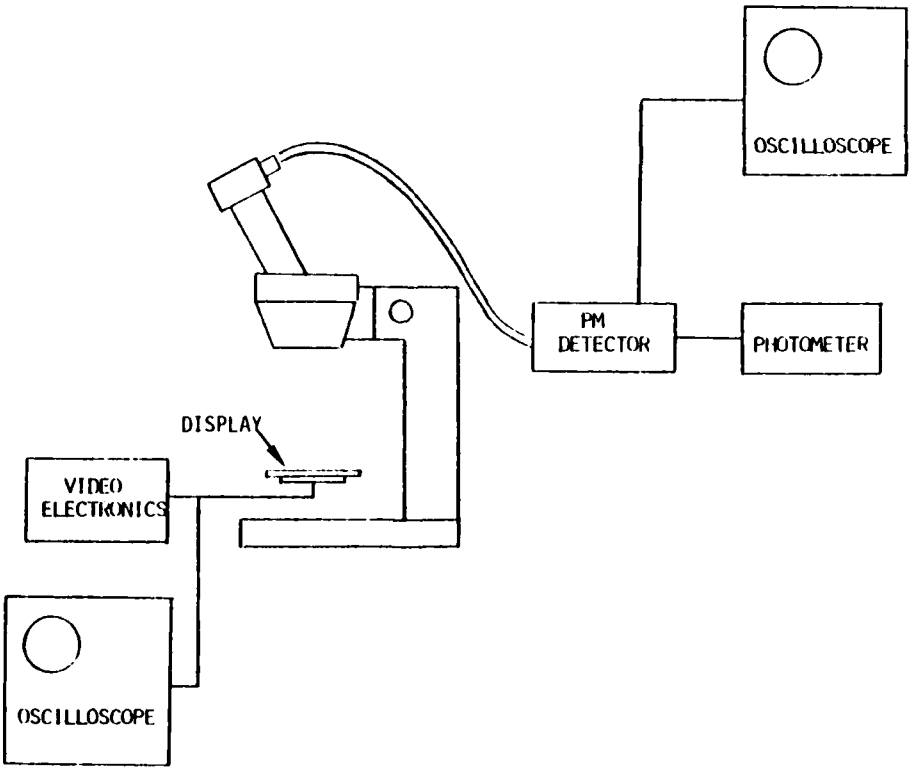


Fig. 5.3-1 Electro-optic test setup.

The required 0.2% duty cycle pulse is generated in the video electronics. The variable width (4-25 μs) pulse is applied to all the columns simultaneously during one-half of horizontal line time (~ 26 μs) and during the second half of the horizontal line time a constant width pulse of opposite polarity is applied to the row. The composite pulse is prepared every 33 ms. During a horizontal line time, only 32 samples are made with the A/D converter since the breadboard display has only 32 columns. During the 33 ms that the rows are normally addressed, only the first 32 are actually addressed and the remainder of the time these rows are in a high-impedance state. This represents 1/500 duty cycle at 30 Hz repetition rate. All measurements were made under these conditions with various patterns created by applying the appropriate video input signals.

The optical sensing system consists of a Bausch & Lomb Model AVB-73 microscope with a Gamma scientific fiber optic eyepiece (Model 700-10-37A). This eyepiece has a 450 μ aperture fiber capable of measuring a single 25 μ square micron cell in the display. The fiber optic eyepiece is coupled to a photomultiplier tube (Gamma Science Model PM101) through a fiber optic pipe. The output of the photomultiplier tube is read by a photometer (Gamma Science Model 2400) for time average brightness measurements. The photomultiplier detector has a photo-optic filter matched to the sensitivity of the photomultiplier tube so that the resultant brightness readings are directly in foot-lamberts.

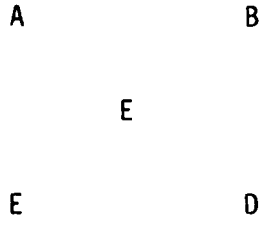
The requirements and goals for this contract are contained in Section 3.0.

5.3.1 Pixel Uniformity

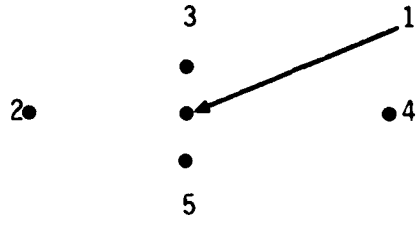
The time average display brightness was measured through the microscope so that the measuring probe sensed the light from just one emitter cell. The matrix was operated at full brightness. The measurement was made in the center and at the four corners. At each measuring position, the center element, as well as the element directly to the left and directly to the

right, directly above and directly below of that center element, was measured for time average brightness. These data are shown in Table 3.2-1. $\Delta B/B$ is also tabulated for each position. B represents the average brightness for the five points at a particular location. The maximum $\frac{\Delta B}{B}$ of 0.237 (24%) is less than the 30% maximum requirement (Sec. 3).

Table 5.3-1
Microuniformity



Measurement position on display



Microlocation within a position

	Brightness - Arbitary Units					
Position	1	2	3	4	5	$\Delta B/B$
A	1.15	1.25	1.33	1.17	1.34	0.152
B	0.65	0.72	0.78	0.62	0.82	0.237
C	0.73	0.72	0.61	0.73	0.70	0.172
D	0.57	0.59	0.49	0.54	0.54	0.147
E	0.80	0.81	0.92	0.83	0.84	0.143

Microuniformity $\frac{B_{MAX}}{B_{MIN}} = 2.7$

(Maximum Overall Variation)

DISPLAY DRIVEN AT MAXIMUM BRIGHTNESS WITH PULSE WIDTH MODULATION

5.3.2 Overall Display Uniformity

Based on the data of Table 5.3-1, the ratio of the maximum to the minimum brightness for 25 data points on matrix 12128 was 2.7, which is somewhat greater than the requirement (2.0) for this particular display.

5.3.3 Contrast Measurement

A contrast measurement was made on 32 × 32 matrix array. The top 16 lines were energized to maximum brightness, the bottom 16 lines were minimum brightness. The brightness was measured from a spot 450 μ in diameter. The measuring spot was moved away from the group of lighted lines. Table 5.3-2 indicates the ratio of the brightness at the center of the edge line (B max) to the measured brightness for several positions away from the lighted area. The ratio B max/B is the contrast ratio. At a distance of one element away, the contrast ratio is 12.5. Table 5.3-3 is a measure of the contrast ratio for a checkerboard pattern (Fig. 5.3-2). The measurement was made by measuring the brightness of a bright spot then moving away into the dark region. Table 5.2-3 shows the contrast ratio at various points on the display. Since a contrast ratio of 11.3:1 is necessary to show eight shades of gray, it can be seen that the display should be capable of at least eight shades of gray as contained in the requirements.

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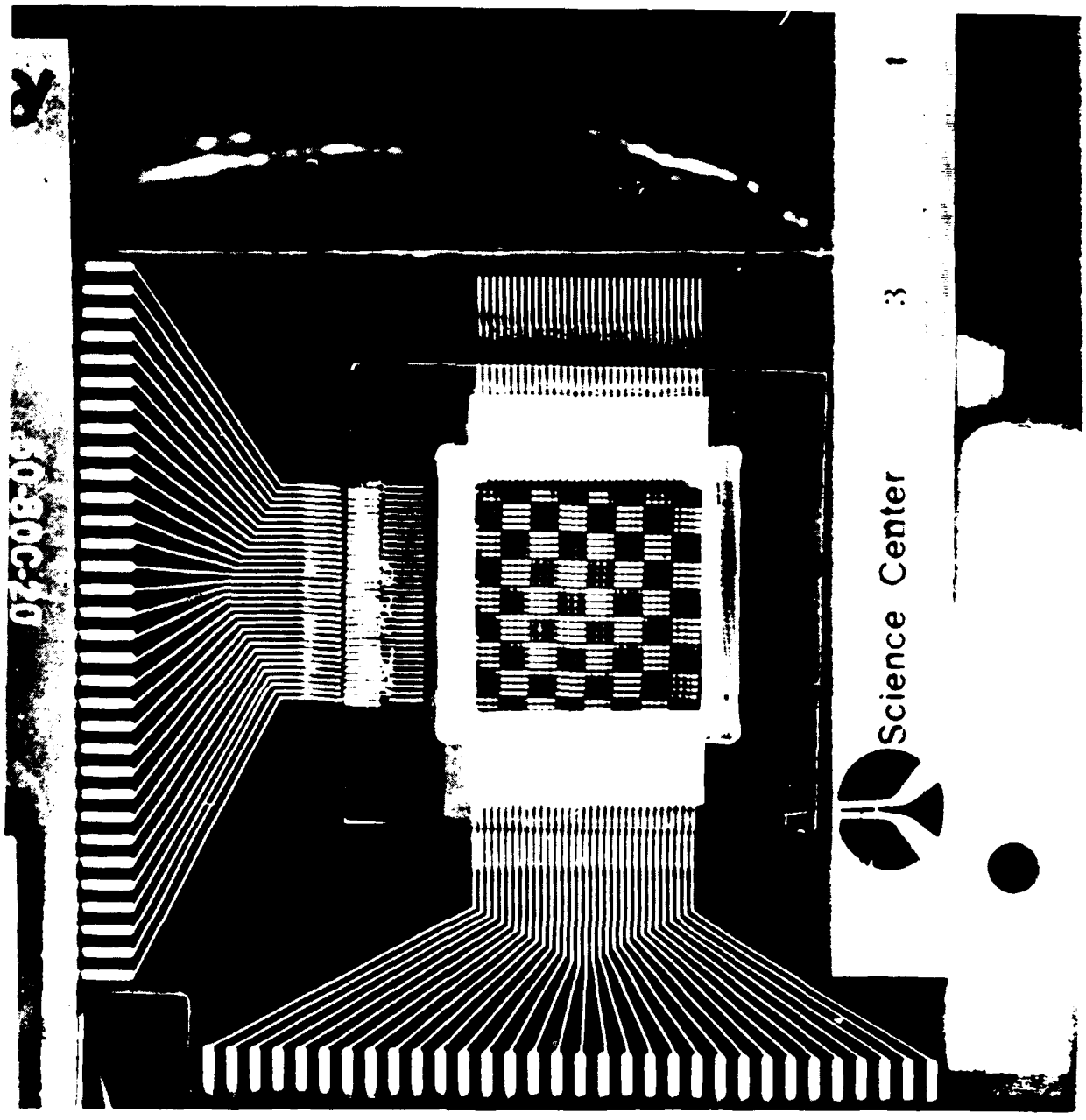

Fig. 5.3-2 Checkerboard pattern 32 × 32 display.

Table 5.3-2

Contrast Ratio Measurements

Top Half of Display Maximum Brightness
Lower Half of Display Minimum Brightness

Distance Away From Bright Cell (in.)	Brightness ft.L	Contrast Ratio
0.000	3.24	
0.003	0.26	12.5
0.066	0.22	14.7
0.099	0.19	17.1
0.1321	0.16	20.3
0.165	0.13	24.9
0.198	0.12	27.0

Table 5.3-3

Contrast Ratio (C.R) Measurement
Checkerboard Pattern

A B

E Display

C D

Position on Display

Distance from Bright Cell (in.)	A ft.L	C.R	B ft.L	C.R	C ft.L	C.R	D ft.L	C.R	E ft.L	C.R
0.000	2.52		1.99		2.03		1.98		2.27	
0.033	0.15	16.8	0.10	19.9	0.17	11.9	0.19	10.4	0.2	11.4
0.066	0.13	19.4	0.10	19.9	0.20	10.2	0.18	11.0	0.19	11.9
0.099	0.13	19.4	0.07	28.4	0.21	9.7	0.18	11.0	0.18	12.6

5.3.4 Gray Scale

Shades of gray are generated in the display by varying the width of the pulse applied to the columns. The nonlinearity of the brightness vs voltage curve was corrected for in the electronics with a nonlinear clock. A staircase waveform is applied to the input of the video electronics in order to generate a shades of gray pattern (Fig. 5.3-3). Table 5.3-4 shows the results of measurements on this pattern. The second column is the measured values and the third column is the calculated values for a change of $\sqrt{2}$ in brightness level for each shade of gray.

Table 5.3-4
Shades of Gray Measurement

Shade of Gray	Measured Brightness (ft.L)	Calculated Value
8	0.54	0.54
7	0.31	0.38
6	0.28	0.22
5	0.21	0.20
4	0.11	0.15
3	0.08	0.08
2	0.04	0.06
1	0.02	0.03

5.4 Power Measurements

Table 5.4-1 shows the power distribution for the breadboard video electronics. These measurements were made with the entire display at maximum brightness. Also shown in the same table is the estimated power requirements for the final prototype.

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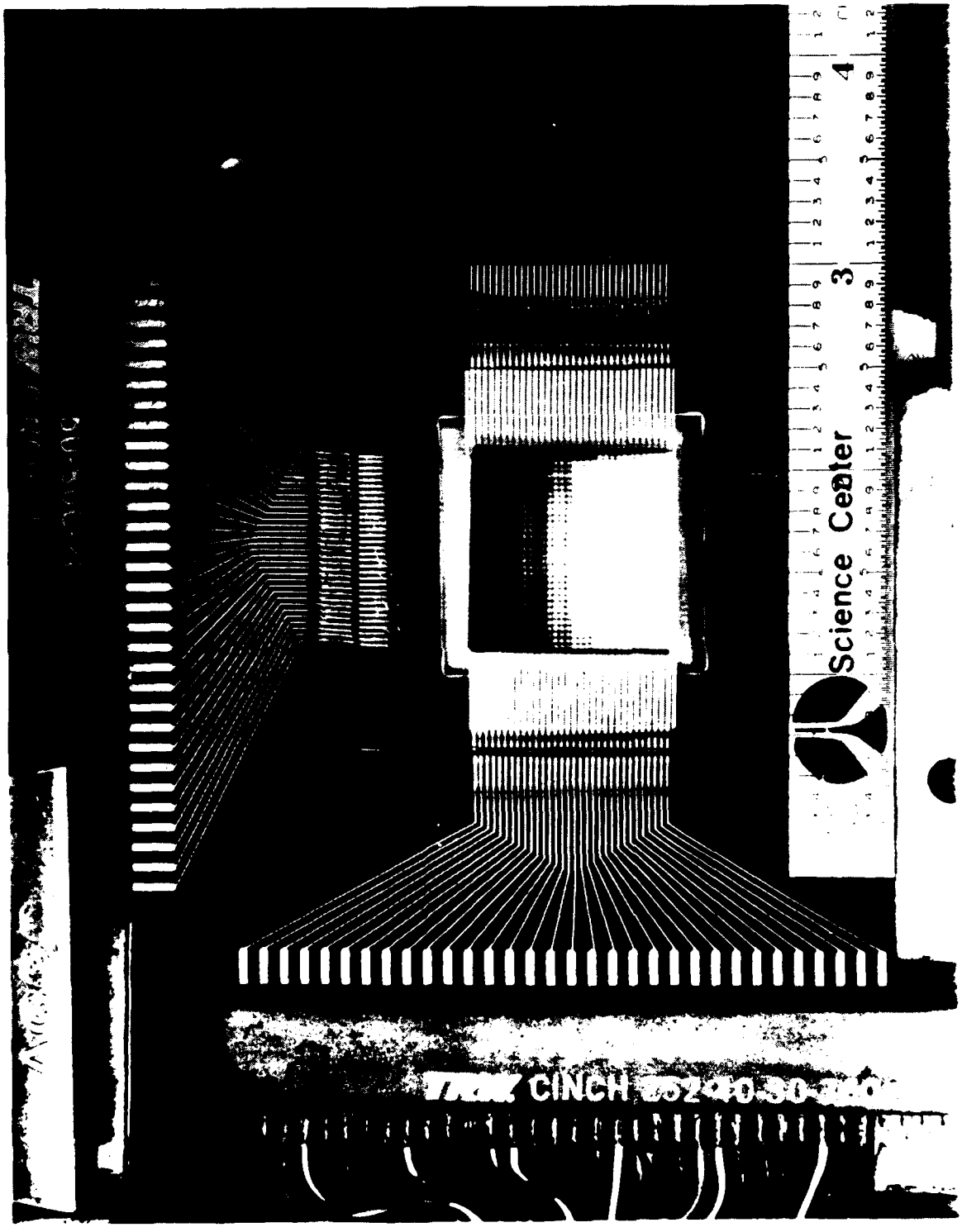

Fig. 5.3-3 Shades of gray pattern.

Table 5.4-1

Power Requirements-100 × 100 Breadboard System

	Breadboard Measurements (Watts)	Semicustom CMOS Final Prototype-(Estimated Watts)	Custom CMOS (Estimated Watts)
A/D	2.250	1.000	0.500
Sync Sep.	0.138	0.100	0.010
Sync Gen.	0.239	0.010	0.005
Control Logic	1.300	0.330	0.100
Shift Reg. Col.	0.660	1.000	0.125
Shift Reg. Rows	0.002	0.100	0.010
Drivers Col.	2.025	0.700	0.700
Display		0.450	0.450
Total Power	6.610	3.690	2.200

The total power consumed by the electronics in the final version was estimated to be approximately half that of the breadboard model. This power savings could be accomplished, in general, by using integrated circuits in place of discrete or small scale integrated devices. Using integrated circuits reduces the number of devices and also saves on area in the hybrid layout. By using semicustom CMOS integrated circuits for most of the control logic and shift registers, and using lower supply voltages, a significant power savings should be realized. Further power savings could be realized in the A/D, shift registers and high-voltage driver.

An alternate approach to lowering the power consumption of the electronics is to use custom CMOS/SOS technology for the logic control and shift registers. The outstanding characteristic of silicon on sapphire technology is the very small capacitance associated with the circuits. Extremely low power consumption on the order of less than 20 mW is characteristic of CMOS/SOS with static dissipation about a milliwatt per LSI device and gate delays of typically a few nanoseconds. A system clock rate of 13 MHz is well within

the maximum performance capabilities of CMOS/SOS. It is estimated that a CMOS/SOS design will require a total of about 250 mW for the control logic and all shift registers. When this is compared to the semicustom logic approach of about 1.7 W, it can be seen that CMOS/SOS represents a significant power savings. The same technology can be used to make the A/D converter with a power savings of about 500 mW.

5.5 Power Measurements on 320 × 240 Display System

When video modulation column drivers became available from Supertex HV01, Rockwell I&D funds were used to develop a breadboard driver and new miniature display surface. The display was over the same nominal area (1 in.) and contained pixels on a 250 element/in. pitch.

Figure 5.5-1 shows a photograph of the compact breadboard system which includes all power supplies in the 1 in. × 15 in. × 16 in. chassis. The TFEL display head was connected by flex cable. The display itself was set in a test fixture and was contacted by elastomeric backed flex circuit material. Therefore, displays could be changed rapidly or the entire display head could be disconnected from the system by means of the PC edge connectors. A demonstration was made to ERADCOM personnel of the operating system.

A series of power measurements were made on the operating system by measuring the DC power input to each section. Where necessary, a filter network was added in the power line so that the average DC power was measured in spite of current fluctuations as the display operated. Table 5.5-1 is a tabulation of this data. Much of the circuitry was constructed of discrete components with little emphasis on low power operation. For instance, the level shifters used resistor pullup loads. Therefore, also included is an estimated power consumption for a refined design using conventional low power ICs. A major improvement is still possible through further refinement in the HV01 driver IC to avoid a 56K pullup resistor integral to each of the 16 channels in the IC. It is estimated that simple circuit redesign could reduce the total system power (including display) to less than 2.5 W. Refinement of the Supertex HV01 could lower that total figure to less than 1.7 W.

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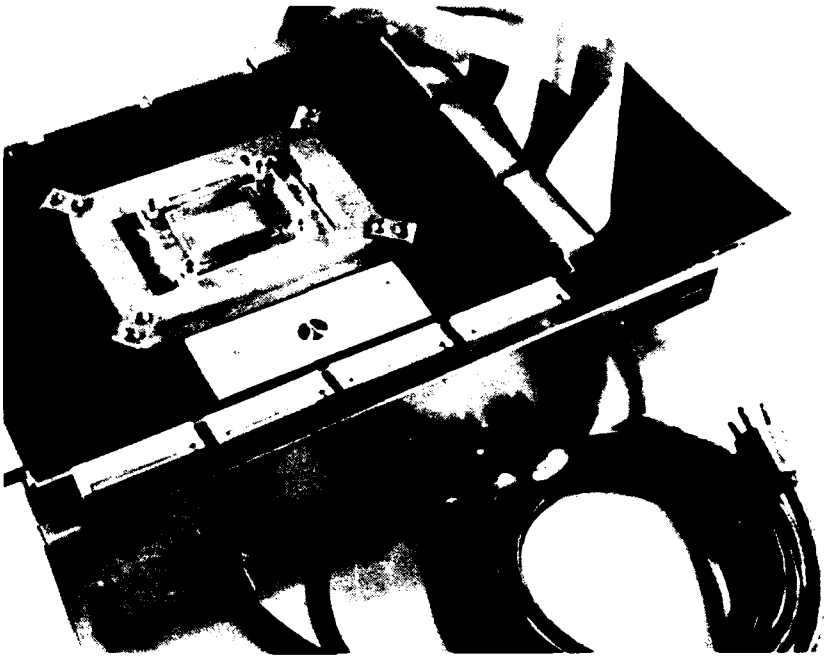

Fig. 5.5-1 320 × 20 breadboard video display system.

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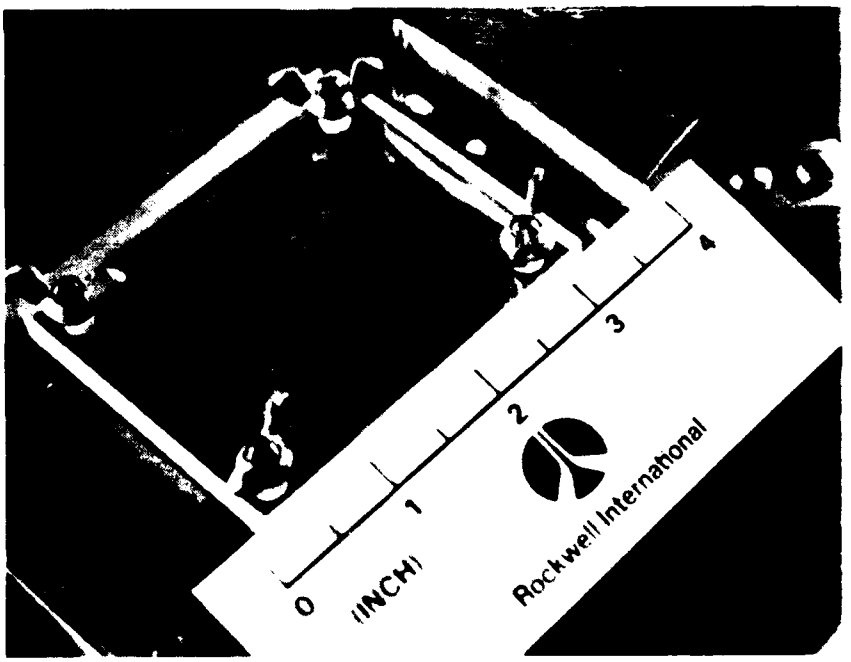

Fig. 5.5-2 Test fixture for 320 × 240 miniature display.

Table 5.5-1

Power Consumption of Miniature TV
Breadboard System (320 × 240)

	Present Power (Watts)	Estimated Power with Circuit Redesign
1. Column drivers - (improved IC - no 56K pullup resistor)	4.83	1.83 0.98
2. Column driver logic	1.95	0.01
3. Line waveform generator	1.35	0.10
4. Level shifters	1.22	0.02
5. Video & sync processing	1.12	0.20
6. Line driver logic	0.46	0.07
7. Timing logic	0.13	0.07
8. Column ramp generator	0.10	0.05
9. Display panel	0.26 max. 0.13 avg.	0.13
Total Power	11.27	2.46 (no spec. driver)
If low power driver IC		1.63 (spec. driver IC)

6.0 HYBRID ELECTRONICS FOR TFEL FLAT PANEL DISPLAY

The following describes efforts at implementing the driver electronics using semicustom logic chips which were intended to couple to the high voltage output driver transistor arrays. As described previously, many of the functions of the logic ICs were incorporated into the driver chip eventually by Supertex. However, this section does document work done under the contract in providing a hybrid driver.

6.1 Method of Approach

The size and weight requirements of the TFEL Flat Panel Display required a densely packaged integrated circuit type of construction. The total volume requirements for the package was 45 × 55 × 12.5 mm. The electronics, which are described in detail in an earlier section of this report, required a substantial number of integrated circuits to perform all of the necessary functions in digitizing the video signal, addressing and driving the display. In addition, a novel interconnection method was required for interconnecting the driver elements to the display rows and columns involving 1195 driver interconnections for the 520 rows and 690 columns. Since the TFEL Flat Panel Display must be portable and capable of battery operation, total power consumption for all circuitry must be kept within several watts.

Fig. 5.1-1 shows a block diagram of the initial approach to the video display electronics. The video information is digitized and addressed to the 683 columns through a series of shift registers, latches, comparators, pulse width modulators, and high-voltage column drivers. A row-sequencer drives the 512 rows as the video information is fed on a row-by-row basis on a 2:1 interlace scanning system as in conventional television.

The meet size space and power requirements semicustom CMOS integrated circuits were developed for the logic functions. These CMOS semi-custom chips are available from any one of several vendors with lower cost, shorter design

and delivery times than those available on fully customized integrated circuitry. The driver chips were a custom development.

To accurately estimate size, space and power requirements, a tabulation of the integrated circuits required, as well as the area of each chip, power consumption estimates and interconnection area allowances for each IC via wire bonding are shown in Table 6.1-1. Also estimates for the required integrated circuits, as well as an estimate for the area required to provide conductor routings, are included as follows:

1. Ground
2. Logic voltage supply
3. Driver high-voltage supply
4. Signal routings
5. Driver-to-display interconnection

Table 6.1-1

Hybrid Area/Power Requirements

Function	Die Size Mils	No. Outputs Per Chip	Total No. of Chips	Avg. Pwr. Watts	Chip Area in.^{2}/chip	Total Area Estimate Σ Chip Area	Total Area Estimate + Incl. Bond Interconnect
Column Shift Reg. Comparator	175 × 175	13	44	1.000	0.0306	1.3464	2.27
Row Shift Regulator	175 × 175	44	12	0.100	0.306	0.3675	0.6075
Display Driver-Col.	80 × 100	16	86	0.700	0.008	0.688	1.9264
Display Driver-Row	80 × 100	16	64	0.450	0.008	0.512	1.4336
A/D Converter	140 × 140	1	1	1.000	0.0196	0.0196	0.0361
13 MHz Clock	100 × 100	1	1	0.200	0.010	0.010	0.0225
800 KHz Clock	100 × 100	1	1	0.030	0.070	0.010	0.0225
Subtotals				3.32 *		2.954 in.^{2}	6.28 in.^{2}
Additional Area Allowance for Conductor Routing, Signals, Power GND, etc.							6.00 in.^{2}
Total Area Requirements							12.28 in.^{2}

Total Area Available - 11.4 in.^{2} (4 substrates 1.5" × 1.9" each)
Area Required for each of 4 substrates - 1.52 × 2.02 (Each substrate = 38.5 × 51.4 mm)
* Power estimates for circuitry only and do not include display power consumption estimated at 300 mW additional.

The area requirements for the ICs are based on actual chip sizes under development, as discussed above. This approach required forty-four column shift register comparator chips, 12 row shift register chips, 86 column high-voltage drivers, 64 row high-voltage drivers, as well as single chips for A to D converter and the 13 MHz and 800 KHz clock sequencing systems. A total requirement of 209 integrated circuits for the video display electronics resulted. While the area requirements for the ICs was only 3.75 $in.^2$, allowances for wire bonding and multilayer interconnect increased the area requirements to 7.6 $in.^2$. Additional allowances for power, ground, and signal routing brought the total requirements to 12.3 $in.^2$.

6.2 Mechanical Layout

The area requirements described above were divided between four substrates, two which drive the column elements, while the remaining two drive the row elements in the flat panel display. The area available on the four substrates is 11.4 $in.^2$ in the heat sink portion with additional area in the interconnect regions bringing total area available up to 12.5 $in.^2$. The packaging and density of the hybrid electronics was based originally on obtaining high-voltage complementary pair drivers on a single chip.

Use of complimentary pair drivers was of particular significance since it greatly simplified circuit wiring. The number of wire bonds was reduced from four wires to two wires per driver, resulting in a savings of almost 2,400 fewer wires in the hybrid circuitry. In addition, the interconnect and signal routing were simplified, resulting in two less layers in the multilayer structure of each substrate. For example, the vertical column board required three layers on the multilayer structure, whereas, with separate n- and p-type high-voltage drivers, five layers would have been required at very high density circuitry.

6.3 Hybrid Substrate Design

The requirements for the hybrid circuit substrate can be summarized as follows:

1. Wide temperature capability from -55°C to 250°C.
2. High-resolution conductors (2-mil lines on 4-mil centers).
3. High conductivity conductors with the maximum resistivity of 1 mΩ per square sheet resistivity.
4. Compatibility with die bonding and wire bonding processes.
5. Capability of direct interface to display interconnection without the need for intermediate connector mediums (requires flexible conductors in the area of the display interconnect).

In view of the above requirements, an approach utilizing a copper-clad polyimide material laminated in multilayers to an aluminum heatsink was chosen as a substrate material. The heatsinks were connected to the exterior package for additional heat dissipation capability. The drive signals extended from the aluminum-supported portion of the substrate on a flexible polyimide extension which is interconnected directly to the display.

6.3.1 Artwork Generation

A technique was worked out using the Hewlett-Packard 9835A computer for generating the graphics art work necessary for the high density hybrid surface. Overall checkout plots could readily be produced using the x-y plotter with the computer and enlarged sections produced where conflicts in trace spacing was suspected. Eventually, the data from these plots were used to do a 15X Gerber photoplot. Subsequently, these photoplots were reduced to 1X photographically on chrome glass masks.

In order to aid in layout of the complete system and assure feasibility of interconnecting the various hybrid driver layers, a 5X mockup was constructed using plots generated by the HP plotter for the artwork on paper

and thick cardboard simulating the display surface and/or the volume of the hybrid package.

6.3.2 Fabrication

The copper-clad polyimide films were selectively plated and etched to obtain the desired conductor and hole patterns. The conductors were typically rhodium and gold-plated for excellent wire bonding characteristics as well as providing corrosion protection for the copper conductors. A photograph of a typical selectively plated and etched multilayer substrate is shown in Fig. 6.3-1. Line widths in the figure were typically 0.004" and spacings vary according to circuit density requirements. Spacing as small as 0.002" can be routinely achieved on the polyimide substrate. A polyimide thickness of 0.002" is sufficient to give adequate voltage breakdown protection between layers (14KV) as well as a reasonable layer-to-layer capacitance. Since the polyimide layers are only 0.002" thick, the multilevel bonding was planned by etching appropriately located holes through the polyimide to expose conductors in the various layers. ICs were directly connected to several conductor layers without the conventional multilayer circuits. Figure 6.3-2 is a diagram showing bonding of ICs to a multilayer polyimide substrate.

Figure 6.3-3 shows typical integrated circuits die attached and wire bonded to the polyimide substrate. The transparent polyimide was laminated to an aluminum substrate whose structure can be seen through the polyimide in the figure. The ICs are attached with a thermosetting conductive epoxy and wire bonded by thermosonics using 0.001" gold (Au) wire with 3-6% elongation. Pull tests showed bond strengths of 8-12 g are comparable to strengths observed in typical ceramic thick film circuits with gold thick film conductors and are generally limited to the pull strength of the 0.001" Au wire.

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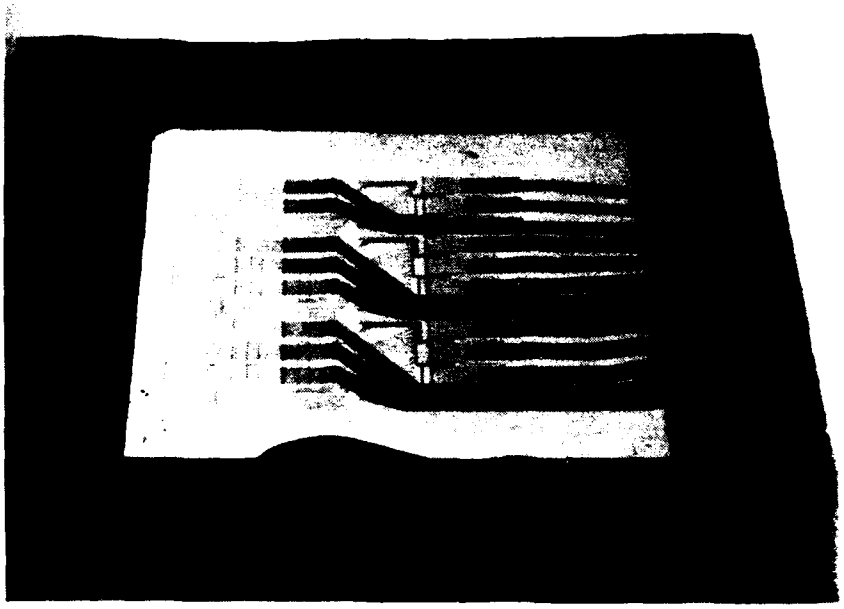

Fig. 6.3-1 Selectively plated and etched multilayer substrate.

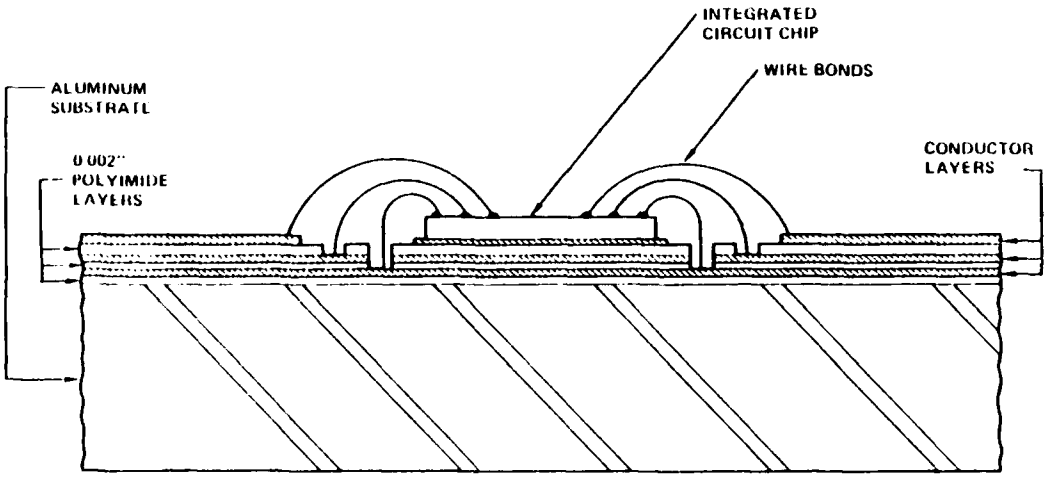

Fig. 6.3-2 Multilayer polyimide substrate.

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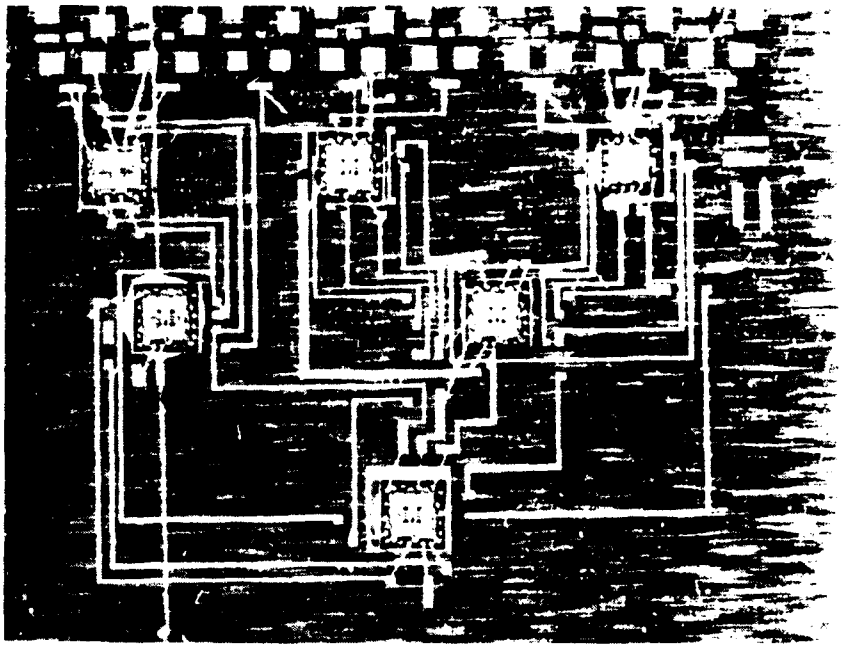

Fig. 6.3-3 Multilayer substrate with ICs attached.

A feature of the polyimide material is the ability to withstand processing temperature (> 300°C) and its stability in various chemical environments as required for plating and processing line traces. However, a disadvantage is the difficulty in providing holes through the polyimide material. Commercially, the holes are normally produced by mechanical punching which is adequate for course resolution PC-type circuits, but not of high enough definition for the current hybrid circuit.

Considerable time was spent in developing techniques for putting holes in the polyimide layer in order to provide vias to lower conductor planes. Most success was obtained using a sodium hydroxide etch. Many resists were tested for use with the sodium hydroxide etch. Success was obtained with a sputtered film of copper appropriately etched with the whole pattern required in the polyimide. Some undercutting did result during the sodium hydroxide etch of the polyimide. A continuing problem was a scum or residue forming around the hole sides so that it was difficult to provide

holes of less than 10 mil lateral dimension. Subsequent work elsewhere has shown that laser evaporation of polyimide material can provide small area holes.

7.0 ELECTRONICS-DISPLAY SURFACE INTERCONNECT

7.1 Rationale for Flex-Circuit Interconnect

The design of this display system uses an electronic driver which is physically separated from the display surface. Since the electronics are not permanently committed to a display surface, either component can be replaced in case of failure. Also, since the electronics are not located on the same plane as the display surface, the frontal area of the display system can be minimized since the electronics can be located behind the display surface. This approach assumes that an easy and reliable technique can be provided for interconnecting all the driver lines (1200 lines) to the display surface. In order that the electronics can be placed at an optimum location with respect to the display, a flexible interconnect system is desirable. Therefore, the test structure utilized a flexible tape cable connecting a rigid substrate simulating the display surface.

7.2 Test Geometry

The test geometry is shown in Fig. 7.2-1. The same pad artwork as used on the display device was used in the contact area of the tape cable. The other ends of the lines fanned out on each side to contact pads on 0.05 in. centers to match a standard edge connector. Both the tape cable and rigid substrate had the conductor pattern of Fig. 7.2-1. In test, the fine pad areas are mated so that continuity and shorts can be measured on the coarse-end pad structure of either part.

Figure 7.2-2 is a photograph of the test setup used to evaluate the interconnect structures. This system is based on the use of a programmable calculator (HP9825A) coupled with a multiline scanning system and digital ohmmeter. The resistance for each of the 50 lines of the pattern shown in Fig. 7.2-1 can be measured using the system in several minutes with a hard copy printout of the resultant resistance for each interconnect line.

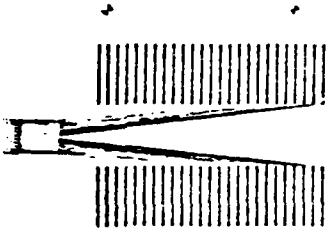

Fig. 7.2-1 Interconnect test electrode pattern.

The tape cable for these experiments was fabricated from copper-clad kapton by conventional photoresist and wet etching techniques. The conductors were nominally 50 μm of 13 μm thick copper contained on a 50 μm thick kapton film. In addition, a rhodium and gold overplate was provided on the copper to avoid oxidation effects at the interconnect. The rhodium prevented intermetallic growth between the gold and the copper. The gold thickness was ~ 2 μm. Reproducing the 50 μm wide line conductor lines in the copper was fairly straightforward. In the case of the glass substrate side, the same pattern was etched in a 5000Å thick evaporated gold coating.

7.3 Elastomeric Bumps

Two different interconnection techniques were evaluated. The first used an elastomeric conductive bump technique (see Fig. 7.3-1). The conductive bump was formed on the glass substrate by stenciling an array of 8 mil dots on 20 mil centers over the contact pads. Prior to stenciling the conductive elastomer on the part, a photoresist insulating layer was applied using Shipley 1350J positive photoresist. The insulating layer had square apertures over the pads to allow contact to the pads. The resist was baked at high temperature in order to assure durability. The insulating layer provided insulation of adjacent circuit traces upon mating the two parts face-to-face (see Fig. 7.3-2).

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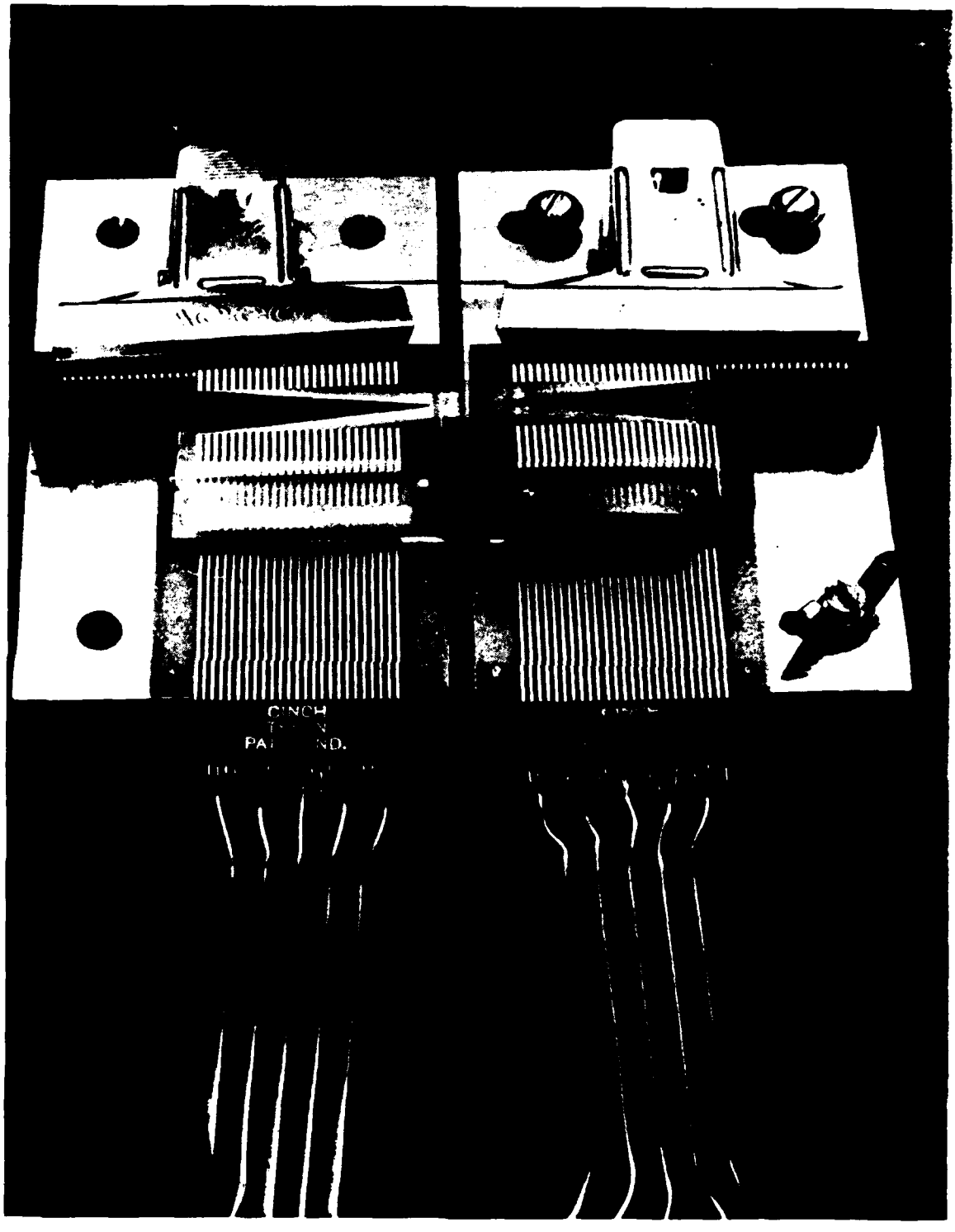

Fig. 7.2-2 Interconnect test setup.

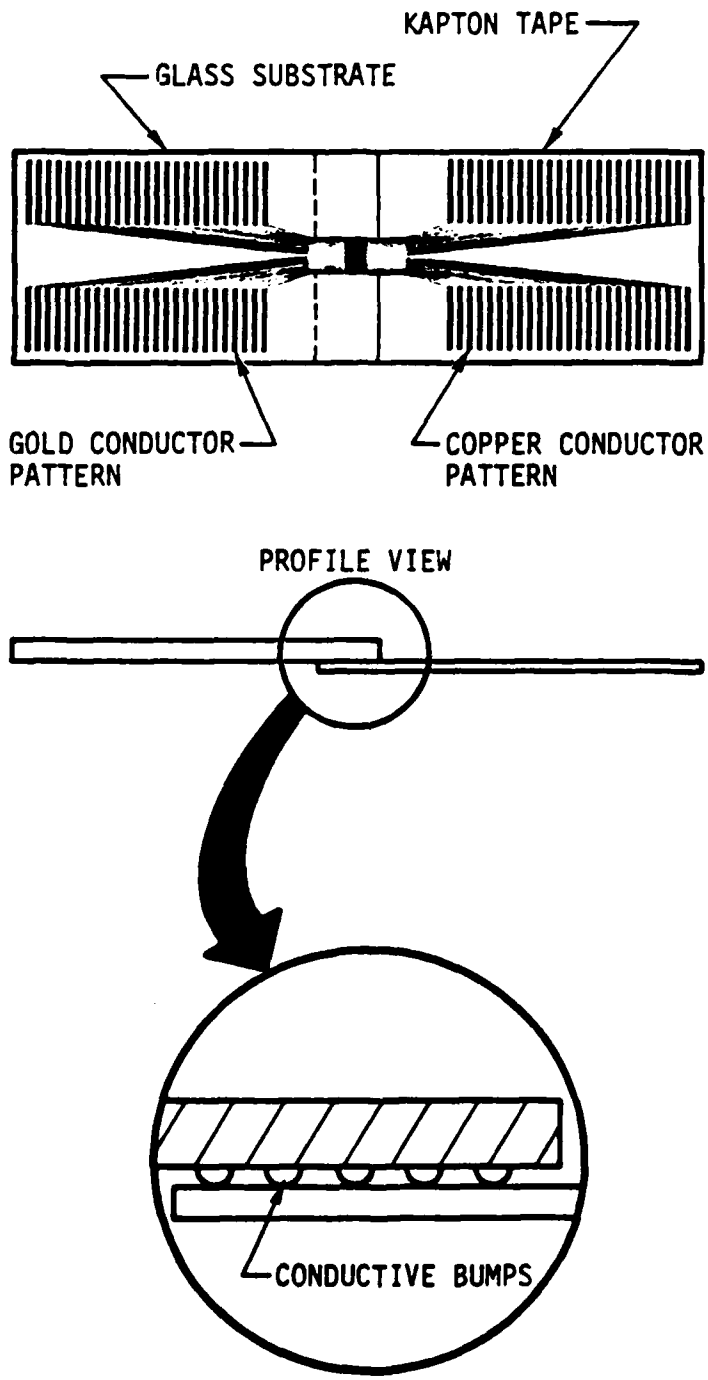

Fig. 7.3-1 Conductive bump interconnect test.

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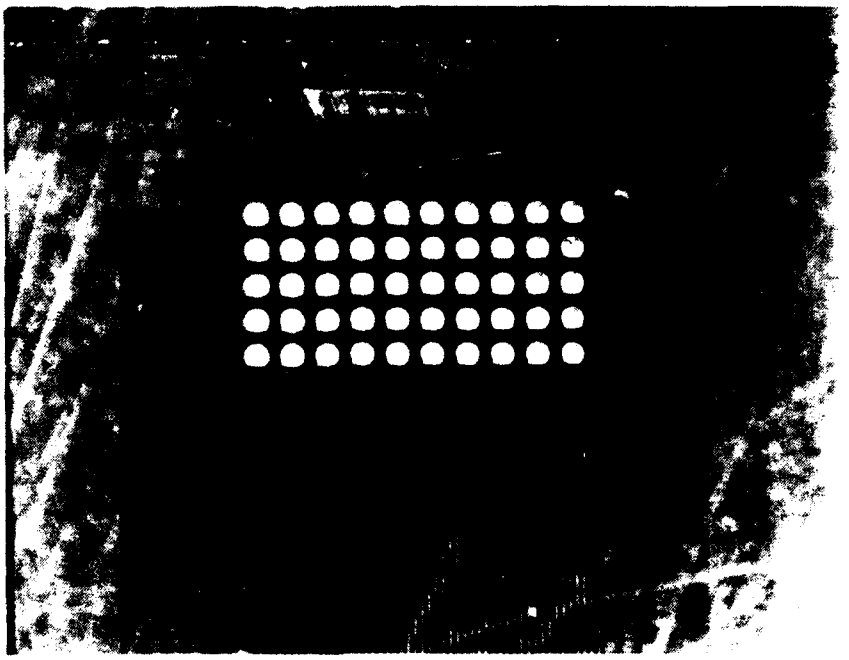

Fig. 7.3-2 Photograph of stenciled bumps.

Interconnection was accomplished by first cleaning the parts meticulously and then with the two parts in contact face-to-face, optically aligning the parts. Finally, a spring C-clamp arrangement held the parts in place. This approach allows easy disconnect, but is subject to mechanical misalignment after the interconnect is made. Also, since the interconnect application does not involve any scraping motion, as is present in a conventional edge connector interconnect, any dirt present such as lint or an oxide film can result in an open conductor path.

The elastomeric conductor material used in these experiments was a urethane filled with 5 μm silver balls. The material had good mechanical properties in that after deformation due to the contacting pressure and release of the parts, the conductive bumps would return to their original profile.

A similar technique was used to interconnect the first parts of the coarse (32 × 32) flat panel displays for the breadboard electronics. Contin-

uing problems were experienced in maintaining reliable contact of low impedance. Therefore, a conductive epoxy and reflow solder joint was finally implemented for the 32 × 32 display. This sort of elastomeric bump connector might be viable for extremely high impedance devices (LCD display) where negligible current is required.

7.4 Evaporated Metal Interconnect

The second approach used an evaporated metal interconnect scheme. In this approach the connections were made directly between the 50 μm lines on 100 μm centers without the use of the conductive pad array. Figure 7.4-1 is a pictorial representation of this kind of interconnect. The conductors on the end of the tape cable are optically aligned with those of the display and the tape is attached to the substrate using a thin epoxy layer under the flexible kapton. Next, a bridging layer of epoxy 1 mm wide overlaps the end of the exposed surface of the tape and the glass substrate to provide a continuous bridge over the sharp edge at the end of the kapton tape. Next, a metal mask 25 μm thick containing 50 μm wide slots on 100 μm centers is optically aligned over the conductors of the tape and the display surface. The slots are ~ 2 mm long. Gold is then vacuum deposited through the mask to provide continuous conductors across the epoxy joint. During the initial cure of the epoxy prior to the gold deposition, the epoxy flows to a feather edge so that there are minimum problems in step edge coverage by the evaporated conductor pattern.

The evaporated interconnect technique results in an exposed conductor surface so that any open lines can be bridged with either ultrasonic wire bonding or a second gold deposition. In the case of lateral short circuits, a laser trimmer can open the short circuits prior to overcoating the lap joint with an epoxy protective layer. Labor involved in the interconnect is minimum since all four sides are connected during one gold deposition. The connection can be removed with epoxy stripper so that a new connection is possible. A further advantage of this technique is that 1/3 less substrate area is required for the interconnect.

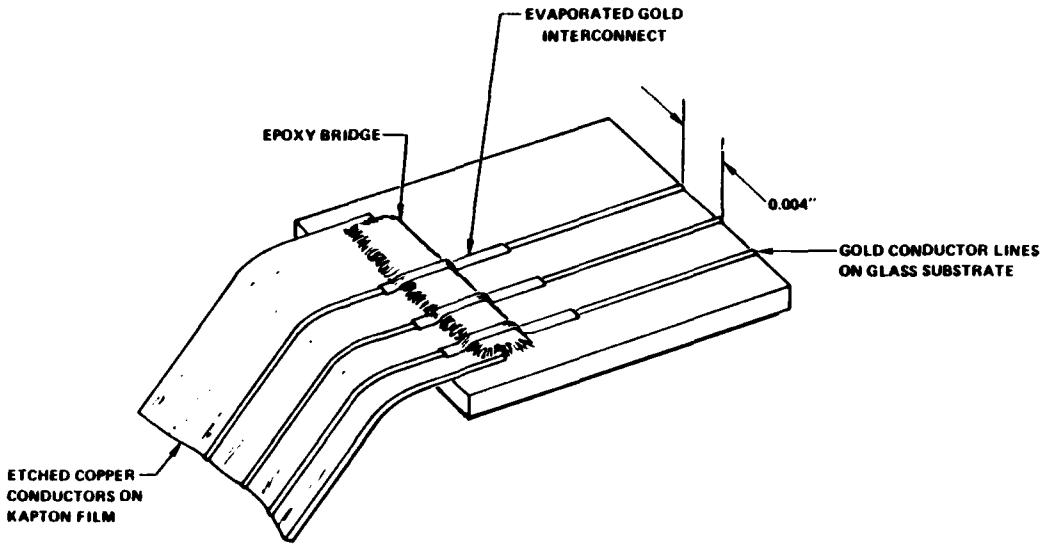

Fig. 7.4-1 High-density interconnect schematic.

Figure 7.4-2 is a photograph of the 50 lead evaporated interconnect test parts. The overall resistance measured in the coarse conductor pads of the interconnected parts varied from 65 Ω to 270 Ω mainly due to the resistance of the thin gold conductor lines; the variation is due to the difference in length of conductor lines to the output pads. Electrical measurement shows a resistance of less than 7 Ω across the 1 mm wide epoxy transition for this type of interconnect. This value is equal to a 1 mm long line of the 50 μm wide gold conductor so that the transition point at the feather edge of the epoxy bridge represents minimum electrical discontinuity (< 1 Ω). A printout of the resistances measured by the test setup shown in Fig. 7.4-2 is shown in Table 7.4-1.

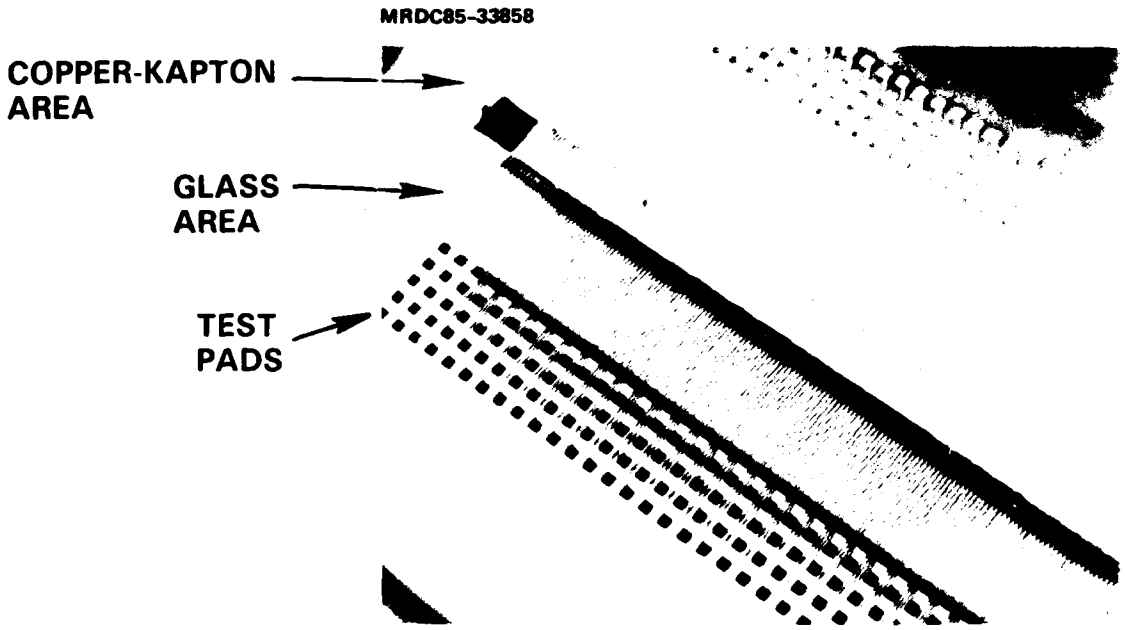

Fig. 7.4-2a Photograph of evaporated interconnect 345 lines (50 μm lines on 100 μm centers).

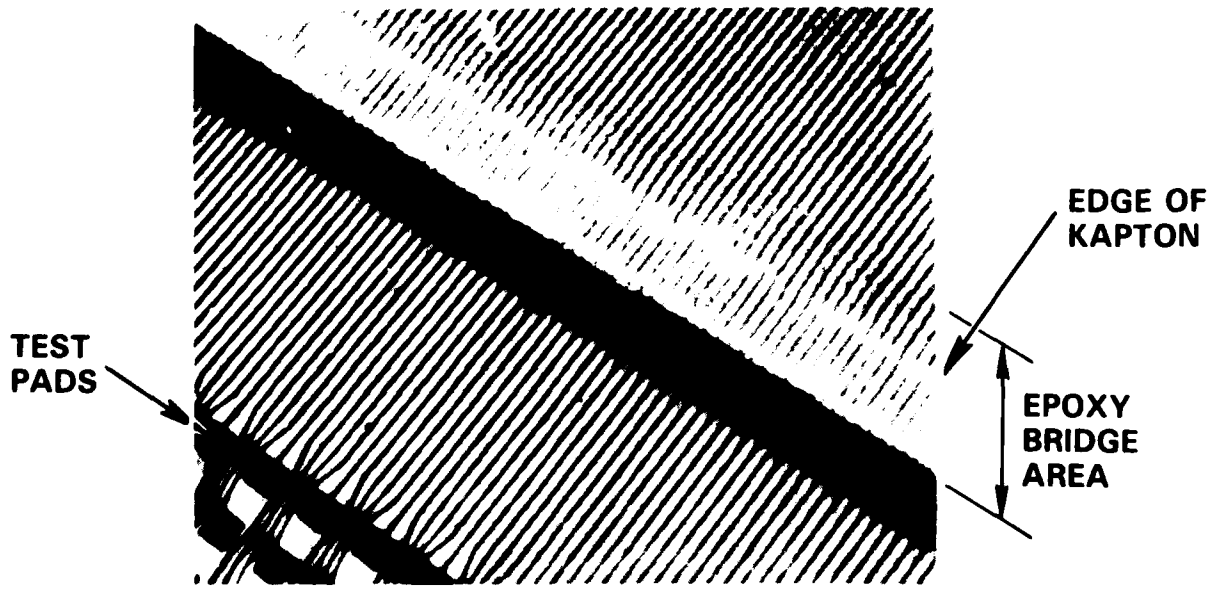

Fig. 7.4-2b Evaporated interconnect-enlarged view of (a) showing expoxy bridge over step edge of kapton.

Table 7.4-1

Resistance of High-Density Interconnect

Column	Resistance of Copper and Gold Lines
1	270.5
2	245.9
3	Open (occurs in etched copper)
4	Open (occurs in etched copper)
5	221.7
6	212.7
7	206.7
8	559.7
9	186.9
10	174.9
11	168.6
12	160.9
13	154.9
14	145.1
15	137.4
16	129.6
17	121.5
18	115.3
19	106.2
20	99.6
21	92.0
22	85.3
23	80.0
24	72.7
25	64.0

In order to be certain that this technique could be used on the full length of the conductor array, (345 conductors over 1.3 in. span) a similar conductor interconnect test was made using the conductor patterns for the display surface. Figure 7.4-2a,b is a photograph of the 345 line interconnect. These tests demonstrated that the metal mask could be fabricated with the required perfection, that the two patterns could be optically aligned with minimum problem, and that the kapton substrate had the required mechanical stability to accommodate the processes involved (photo etching and epoxy cure at 160°C).

As a further test to verify the validity of this approach, a course resolution matrix display (32 × 32) was interconnected using the evaporated metal technique. Since the 32 × 32 display has an equivalent area to the final fine line display, the current density across the interconnect is similar to that of the final system. Tests of the evaporated connections in both the row and the column access lines showed no problems during video addressing of the display. All evaporated interconnects were intact after fabrication without any requirement of repair. Also, the interconnect was made in an area similar to that required on the final fine line display.

We believe that this type of high-density interconnect represents a new technology. U.S. Patent No. 4255613 has been granted on this structure. Conceivably, an extension of this technique could provide a means of connecting the semiconductor chips to the copper conductors on the kapton substrate of the hybrid driver surface and so allow a higher density of chips in the hybrid package as well as reducing the assembly labor required compared with the conventional wire bonding approach.

8.0 CONCLUSIONS

Most of the component parts necessary to provide a truly high density miniature TV display system were successfully developed during this program. These include a high resolution display surface (500 lines per in.), a high density interconnect system (250 lines per in.), as well as techniques for fabricating high density hybrid surfaces on flex circuit material so that the electronics can be located behind the display surface. With the recent availability of high voltage IC drivers this past year, the missing link in fabricating a complete high density TV system is now available.

Based on power consumption measurements of a 320 × 250 breadboard system, it appears that a miniature system can be made with current technology which will consume less than 2.4 W. Reduction in this power consumption could be accomplished by the following:

1. Refinement of the high voltage IC driver to eliminate the requirement for the internal 56K Ω resistance pullup resistor. This should enable a system with less than 1.7 W power consumption.

2. Development of a resonant drive system for recovering the energy of the charge stored in the display surface capacitance. Similar developments for use with a graphics display system has resulted in a factor of three reduction in power dissipation with the display system.[3]

3. Use of CMOS-SOS logic components could further reduce the power requirement.

In terms of further display surface development, the following steps could improve the performance of the system.

1. Development of a redundant address line geometry so that failure of one pixel would not interrupt the address line with resultant failure of part of the line.

2. Optimization of the emitter cell geometry so the emitted light is concentrated in a forward direction with resultant improved display brightness when placed into an optical system.

3. Incorporation of a narrow spectral band emitter such as provided by rare earth activators, so that a lightweight diffraction optics system can be used as the magnifier in a portable display system.

4. Incorporation of multicolor emitters so that a full color display could be generated.

9.0 REFERENCES

1. R.D. Ketchpel, "miniature Active Matrix Display Final Report," Contract No. DAAK70-77-C-0141, U.S. Army Night Vision Laboratory (1978).

2. P. Alt and P. Pleshko, "Frame-Time Analysis of the Performance of Refreshed Matrix Addressed Display," Digest SID International Symposium, pp. 84 (1975).

3. M.L. Higgins, "A Low-Power Drive Scheme for AC TFEL Displays," Digest 1985 SID Intl. Symp., pp 226 (1985).

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